
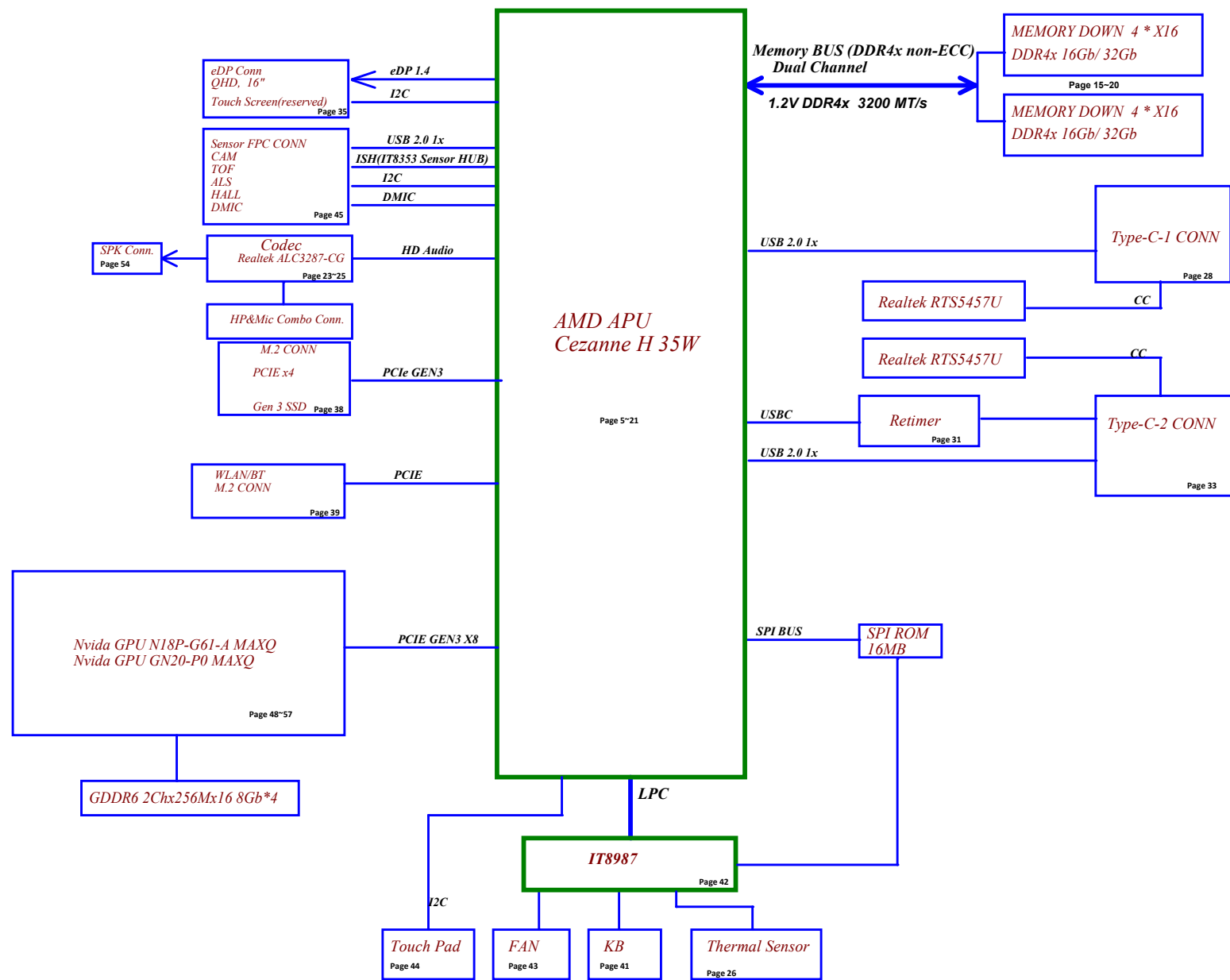


Schematics Page Index (Title / Revision / Change Date)

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12	FP6 POWER	1.0		46	Blank	1.0	
13	FP6 GND	1.0		47	Discharge	1.0	
14	BLANK	1.0		48	Blank	1.0	
15	DDR4 CH A	1.0		49	Blank	1.0	
16	DDR4 CH A	1.0		50	Blank	1.0	
17	DDR4 CH B	1.0		51	Blank	1.0	
18	DDR4 CH B	1.0		52	Blank	1.0	
19	DDR4 (DECAPS)	1.0		53	Blank	1.0	
20	DDR4 TERMINATIONS	1.0		54	BLANK	1.0	
21	Strap Pin	1.0		55	TPM	1.0	
22	Blank	1.0		56	POWER DCIN & BATTERY CHARGER	1.0	
23	USB C Redriver	1.0		57	POWER DELIVERY 3.3V/RTC	1.0	
24	Blank	1.0		58	POWER DELIVERY 5V	1.0	
25	Blank	1.0		59	POWER DELIVERY 1.8V	1.0	
26	Blank	1.0		60	POWER DELIVERY 0P75A 0P75SX	1.0	
27	Blank	1.0		61	POWER DELIVERY-1.2V/2.5V	1.0	
28	Thermal sensor	1.0		62	POWER DELIVERY Load SW	1.0	
29	SYSTEM FLASH	1.0		63	LED Backlight	1.0	
30	TYPE C SINK/SOURCE SWITCH	1.0		64	POWER DELIVERY APU Power	1.0	
31	TYPE C RTS5452E	1.0		65	POWER DELIVERY 1P95V	1.0	
32	TYPE-C CONN	1.0		66	POWER DELIVERY 3.6V WIFI	1.0	
33	USB3.0&2.0	1.0		67	Blank	1.0	
34	BLANK	1.0		68	Debug Conn	1.0	
				69	Hole & Mark	1.0	
				70	Changelist	1.0	

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I2C Allocation Mapping

I2C Allocation Mapping						
EC	Device1		Device2		Device3	
SMCLK0	Type-C1(PD)	0x40	x	x	x	x
SMDAT0						
SMCLK1	Battery	0x16	x	x	x	x
SMDAT1						
SMCLK2	Charger	0xD6	GPU	0x9E	LCD Back Light	0x58
SMDAT2						
SMCLK3	Debug	address:TBD	x	x	x	x
SMDAT3						
SOC	Device1		Device2		Device3	
I2C_CLK0	TOUCHPAD	0x15	X	X	X	X
I2C_DAT0						
I2C_CLK1	TOUCHPAENL	0x10	X	X	X	X
I2C_DAT1						
I2C_CLK2	X	X	X	X	X	X
I2C_DAT2						
I2C_CLK3	X	X	X	X	X	X
I2C_DAT3						
I2C_CLK4	X	X	X	X	X	X
I2C_DAT4						
I2C_CLK4B	X	X	X	X	X	X
I2C_DAT4B						
ISH_I2C_CLK0	X	X	X	X	X	X
ISH_I2C_DAT0						
ISH_I2C_CLK1	X	X	X	X	X	X
ISH_I2C_DAT1						
ISH_I2C_CLK2	X	X	X	X	X	X
ISH_I2C_DAT2						



Huaqin Telecom Technology Com.,Ltd.

Page name: I2C Table

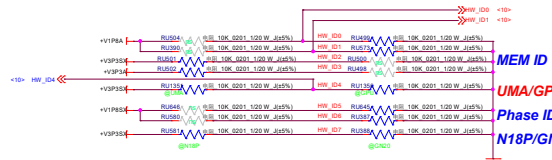
Size: A4	Project Name: NB3029(S560-16ACN)	REV: V1.0
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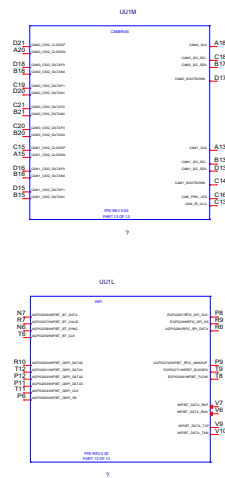
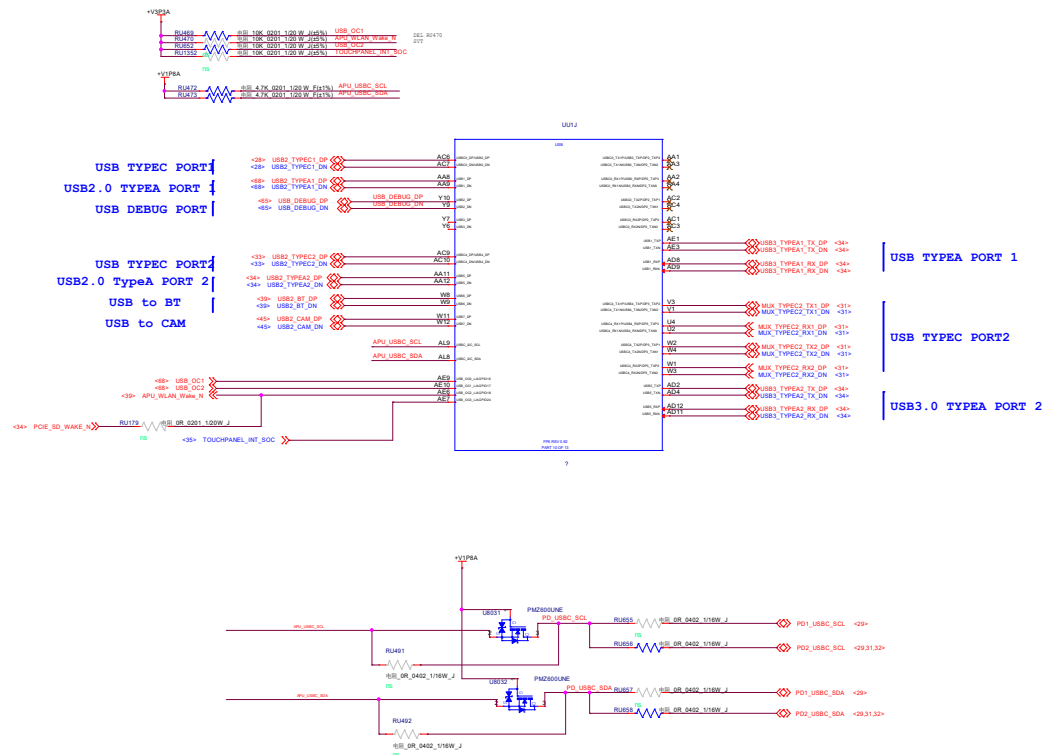
Date: Tuesday, January 19, 2021	Sheet: 4 of 89
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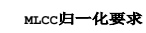
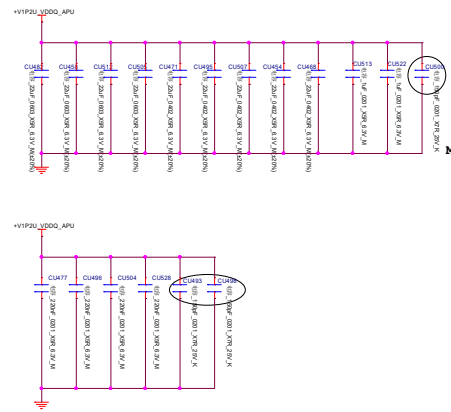
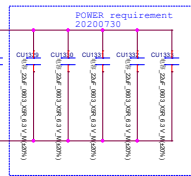
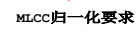
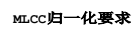
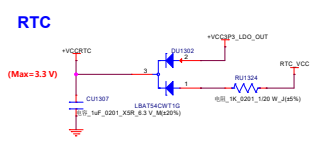
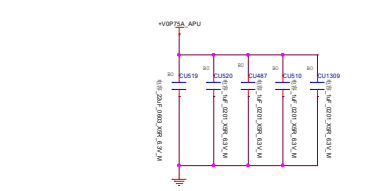
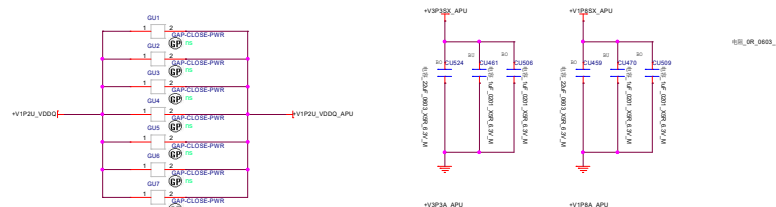


PM_ID0	PM_ID1	PM_ID3	Description	Total
0	0	0	Samsung S6D P448315MC-SCWE	826
0	0	0	Hyundai S6D P33AMG80D7R-KXC	826
0	0	0	Microton S6D P740A512M147B-042R-J	826
1	1	0	Samsung 16G0 P44AG158MA-SCWE	1626
0	0	1	Hyundai 16G0 P33AMG6C8MC-KXC	1626
1	0	1	Hyundai 16G0 P33AMG6C28-KXC	1626
0	1	1	Microton 16G0 P740A51G148D-042R-E	1626
1	1	0	Reserve	TBD
0	0	0	Reserve	TBD
1	0	0	Reserve	TBD

NW_ID5	NW_ID6	Description
0	0	XVT
1	0	FVT
0	1	SIT
1	1	SVT&SOVP

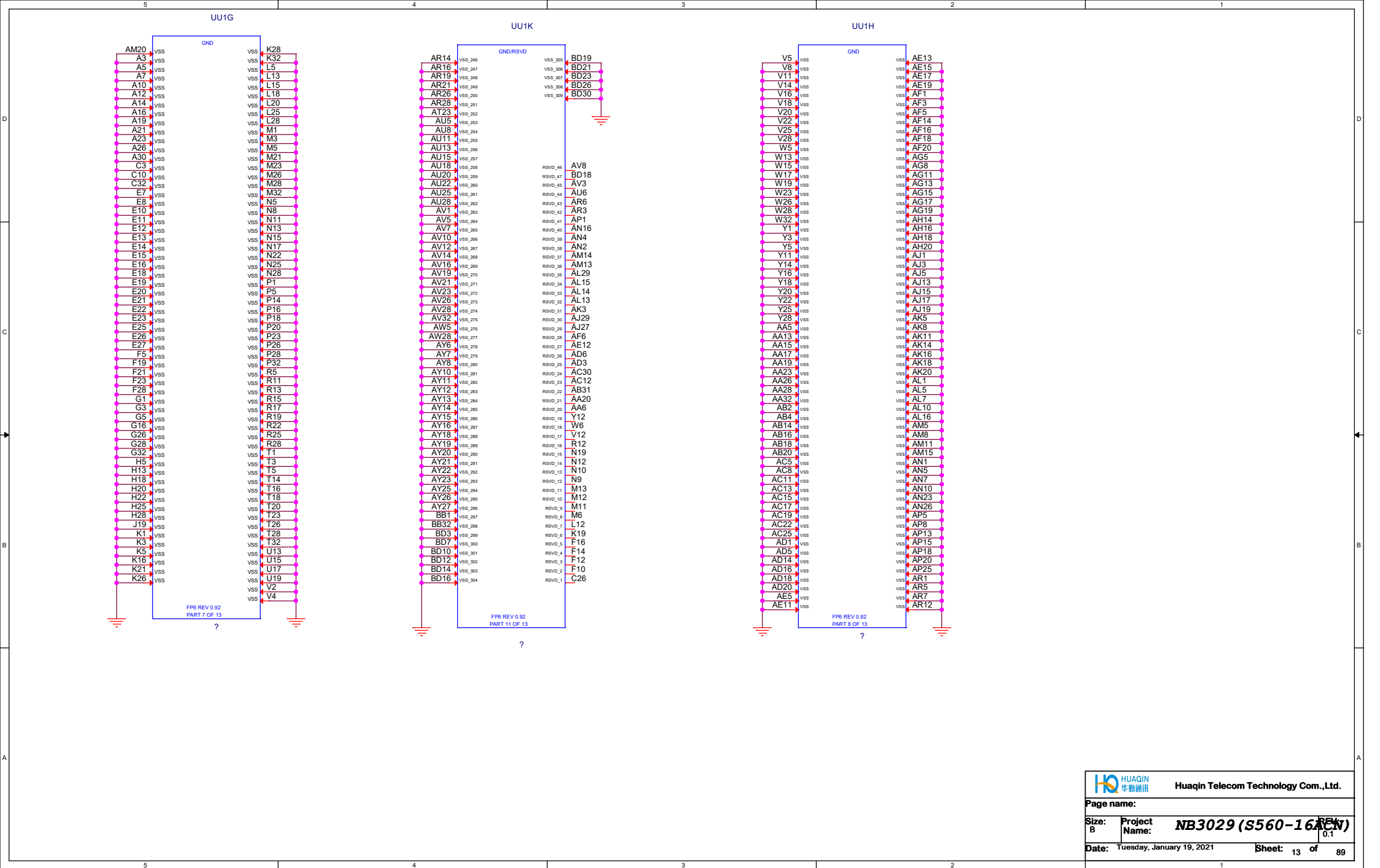


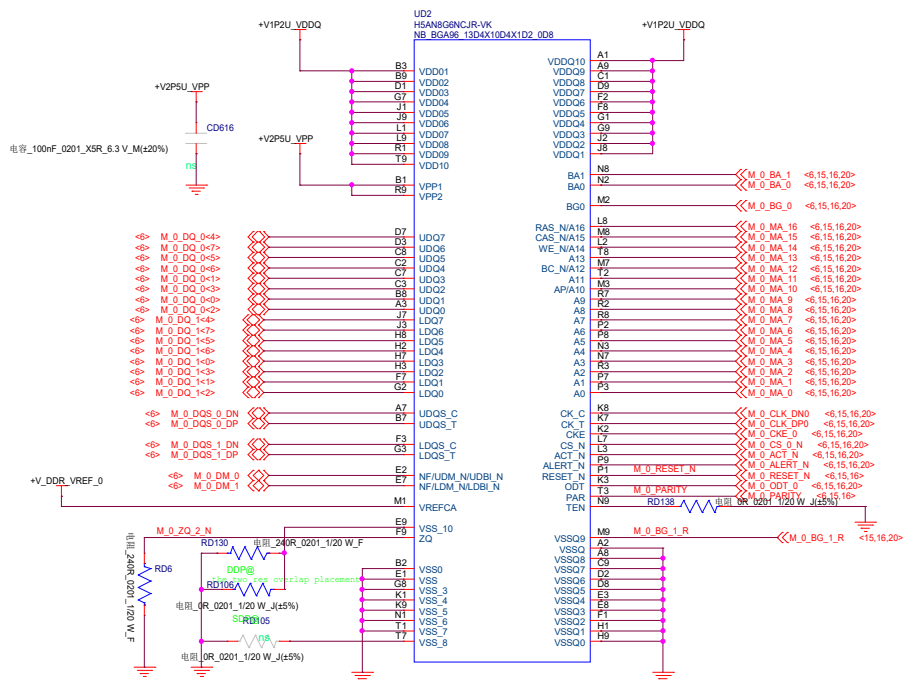




Capacitor		VDDCR	VDDCR_SOC
Value	Package Size / Material		
22 μ F	0603 X5R	168U	7BU
1.0 μ F	0402 X5R	-	1BU
0.22 μ F	0402 X5R	-	-
180 pF	0402 COG NPO	1BU	1BU

Note: B0=Bottom. Under the processor





Close to U01 Pin P1

+V1P2U_VDDQ

CD639 电容 100µF, 0.01 XSR, 8.3V, M4208

CD640 电容 100µF, 0.01 XSR, 8.3V, M4208

+V_DDR_VREF_0 ns

+V1P2U_VDDQ

RD97 电阻 1K, 0.201 1/20 W_F

RD98 电阻 1K, 0.201 1/20 W_F

CD1 电容 100µF, 0.01 XSR, 8.3V, M4208

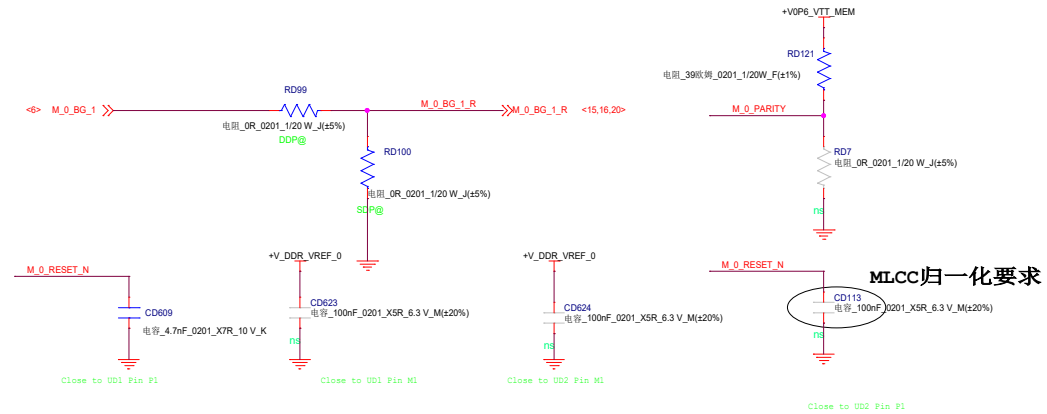
CD633 电容 100µF, 0.01 XSR, 8.3V, M4208

CD683 电容 2.2µF, 0.02 25 V, M4208 ns

CD695 电容 100µF, 0.01 XSR, 8.3V, M4208

+V_DDR_VREF_0

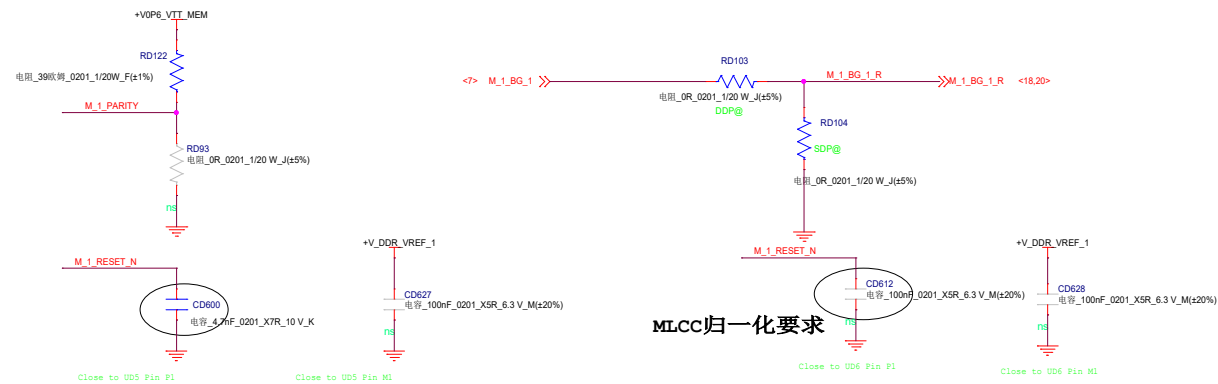
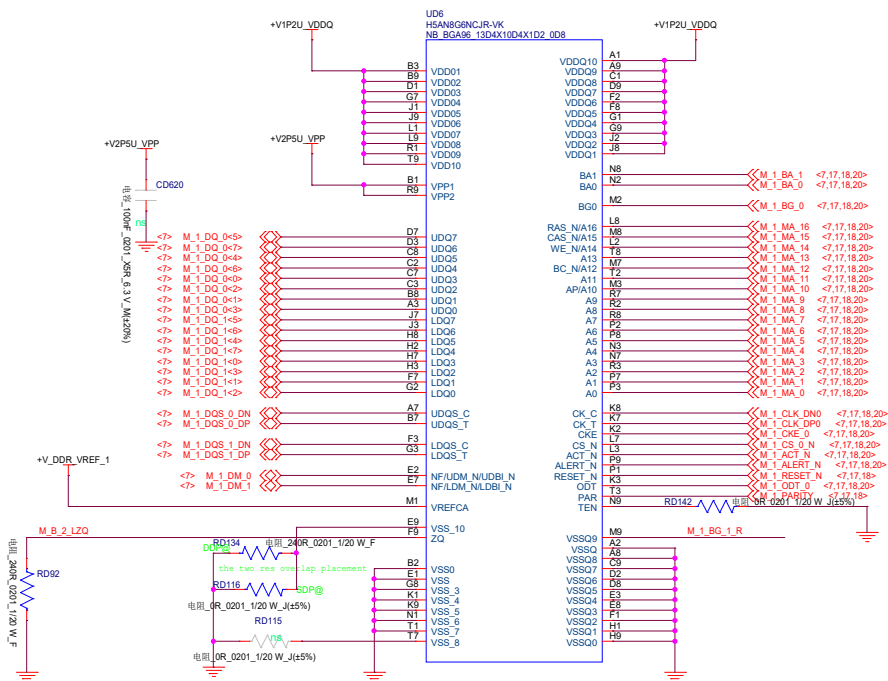
PR APU Change to 1K to VTT 0.6V



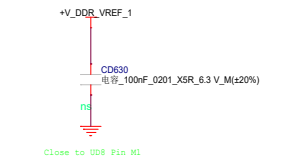
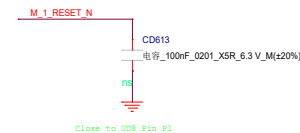
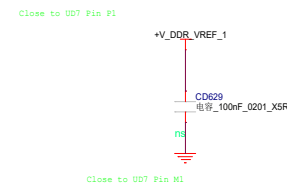
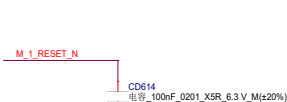
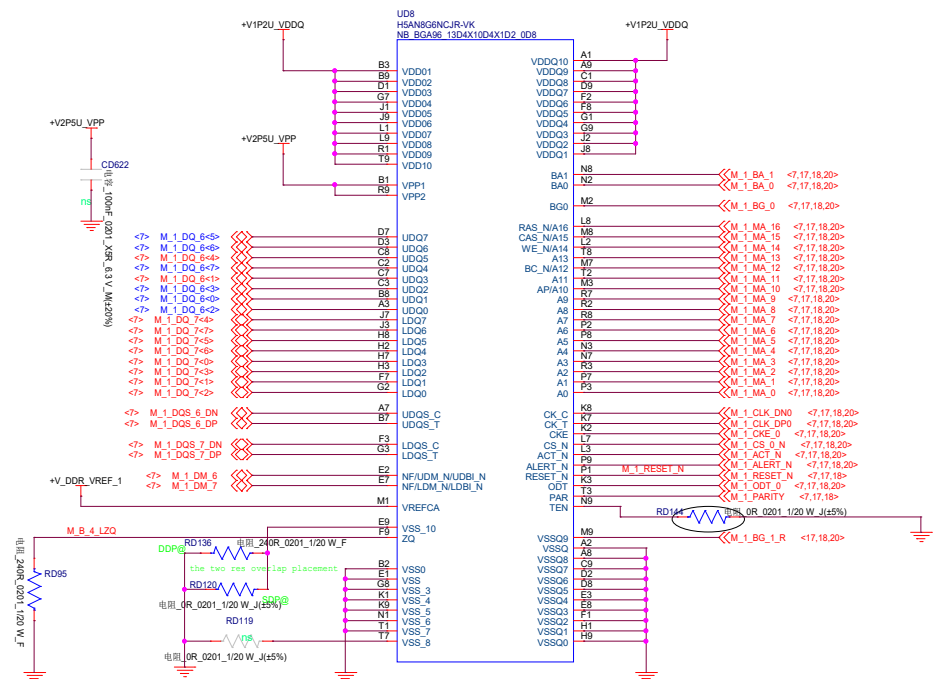
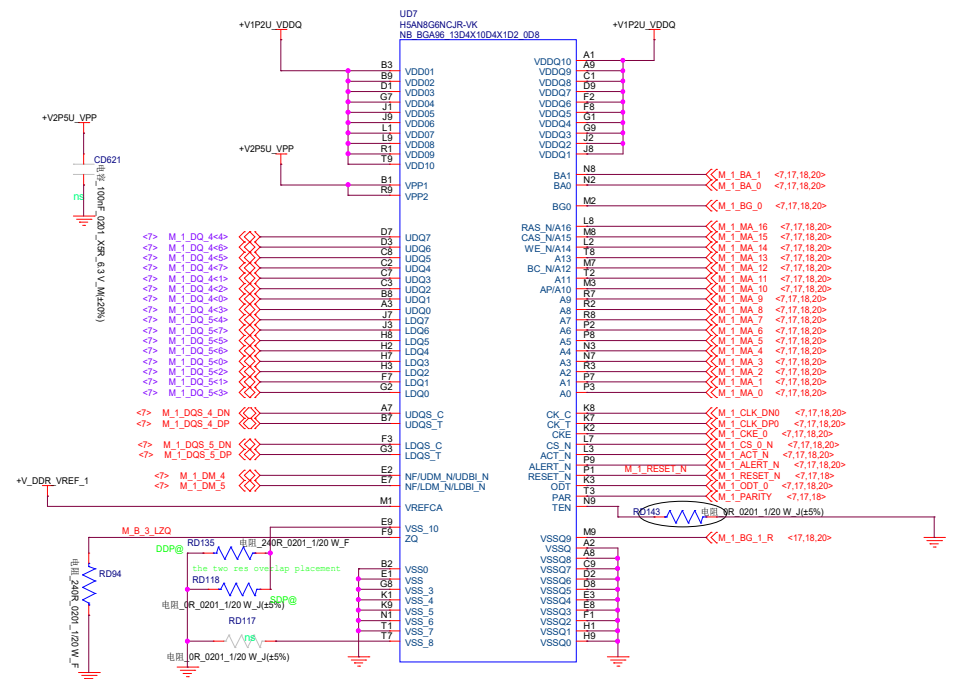
DDR PINS		SDP				DDP			
E9	UZQ	RD108	RD129	RD106	RD130	RD108	RD129	RD106	RD130
		ON	NC	ON	NC	NC	ON	NC	ON
M9	BG1	RD100		RD99		RD100		RD99	
		ON		NC		NC		ON	



Default: **SDP**



DDR PINS		SDP				DDP			
E9	UZQ	RD114	RD133	RD116	RD134	RD114	RD133	RD110	RD132
		ON	NC	ON	NC	NC	ON	NC	ON
M9	BG1	RD104		RD103		RD104		RD103	
		ON		NC		NC		ON	

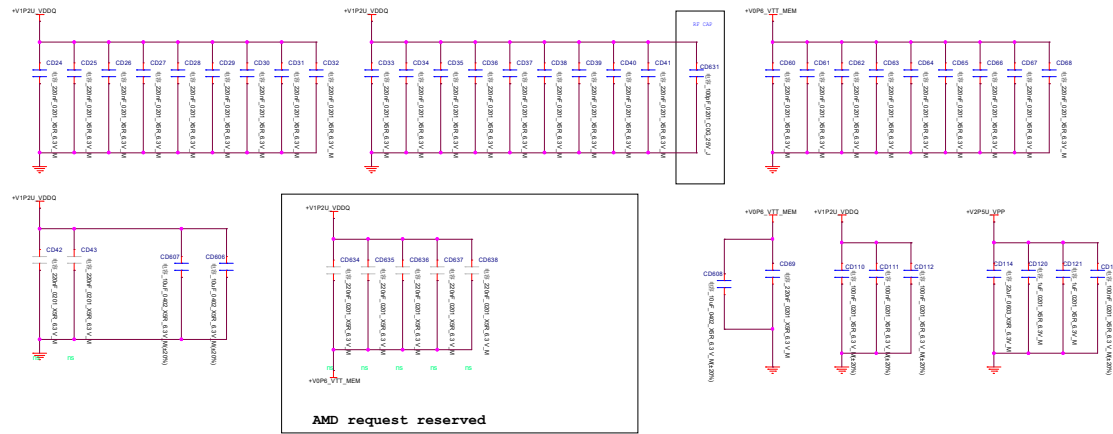


DDR4 CHB UD7 UD8 NOTE

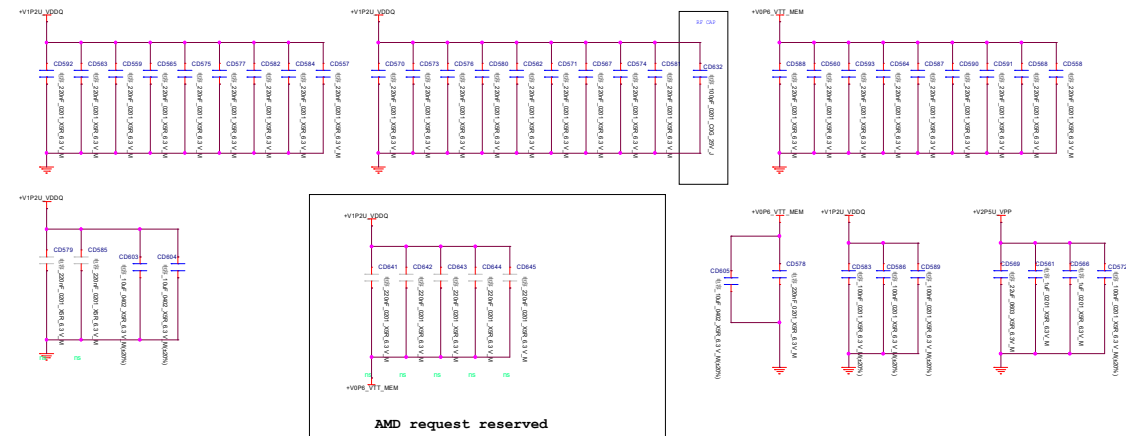
DDR PINS		SDP				DDP			
E9	UZQ	RD118	RD135	RD120	RD136	RD118	RD135	RD120	RD136
		ON	NC	ON	NC	NC	ON	NC	ON
M9	BG1	RD104		RD103		RD104		RD103	
		ON		NC		NC		ON	

Default: SDP

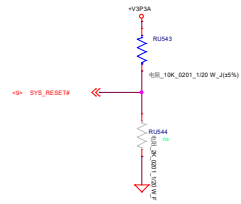
DECOUPLING CAPACITORS FOR DDR CHANNEL A



DECOUPLING CAPACITORS FOR DDR CHANNEL B

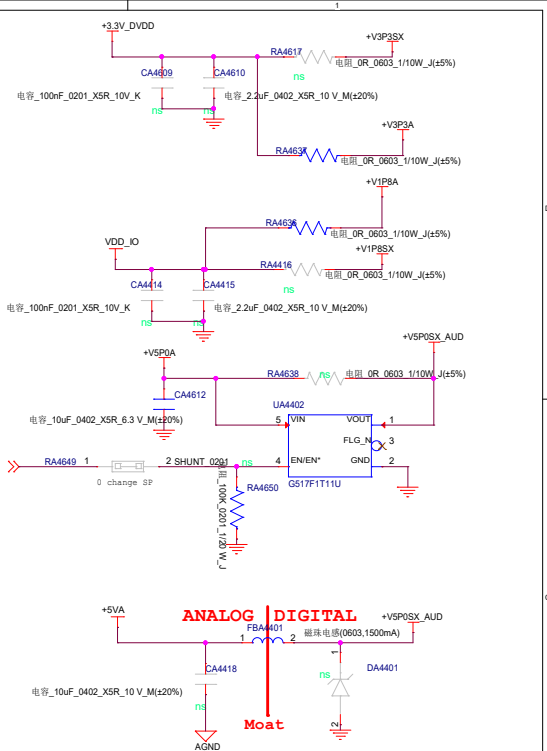
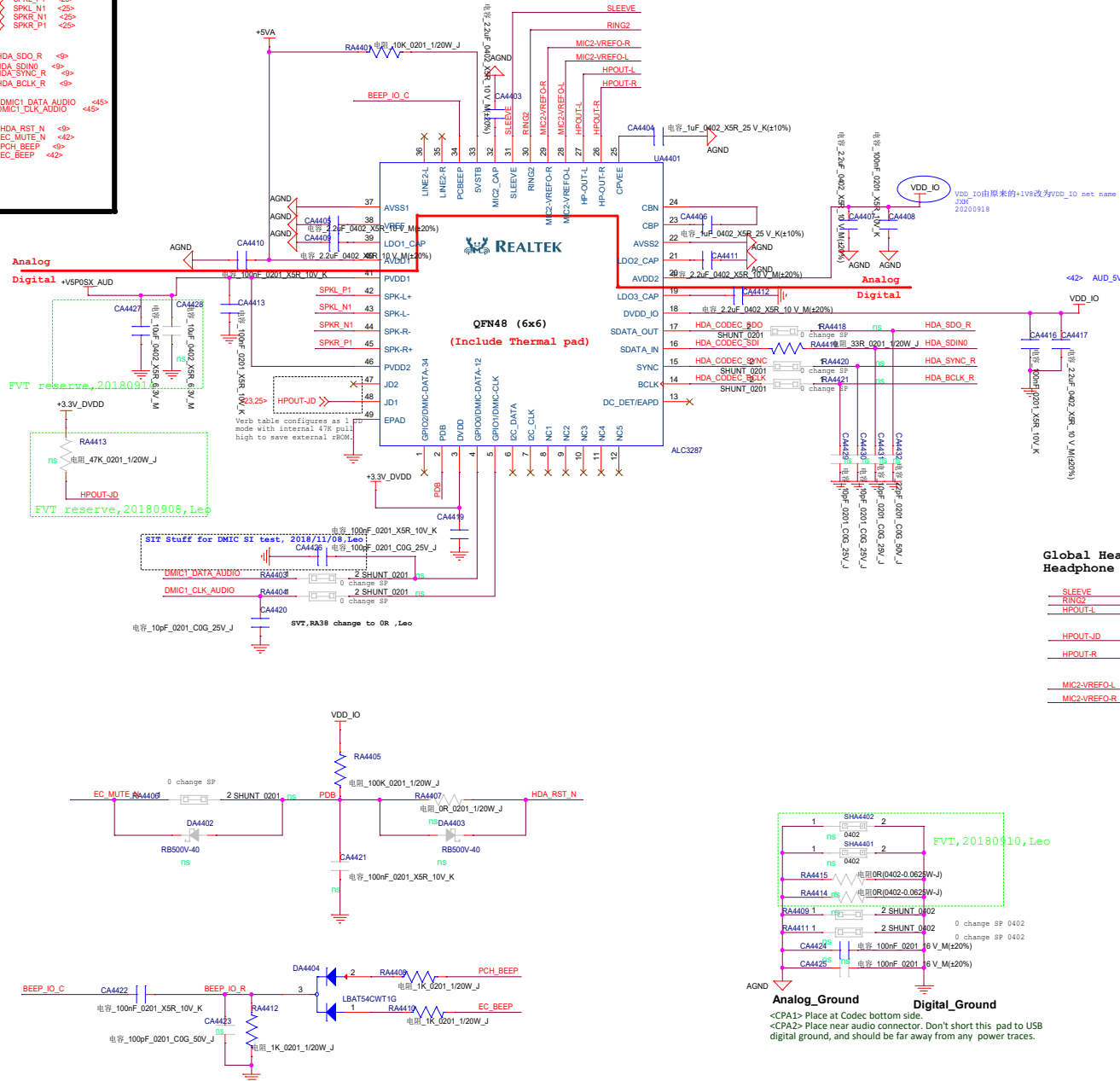
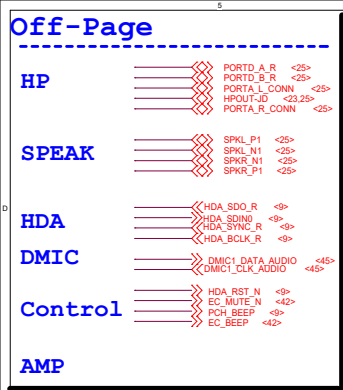


STRAP PINS



SWMP	FUNCTION	DEFINITION
WPL_CLKA		1. USE: BRING ON-TIME CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0. USE: TURNED POKE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
WPL_RESET		1. NORMAL RESET MODE(DEFAULT) 0. SLOW RESET MODE

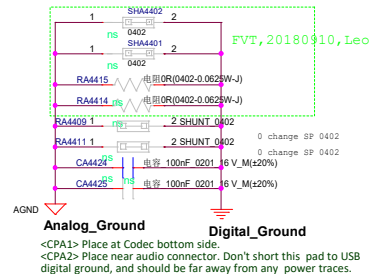




Global Headset Jack with 2Vrms and 120dB SNR.
Headphone / Line Out / CTIA & OMTP



Internal Speaker connector
Placement near Audio Codec
SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils





—	PORTD_A_R	<23>
—	PORTD_B_R	<23>
—	PORTA_L_CONN	<23>
—	HPOUT_JD	<23>
—	PORTA_R_CONN	<23>
—	SPKL_P1	<23>
—	SPKL_N1	<23>
—	SPKR_N1	<23>
—	SPKR_P1	<23>

SPKL_P1_CONN	1	FTP4608	ns	26MIL
SPKL_N1_CONN	1	FTP4607	ns	26MIL
SPKR_P1_CONN	1	FTP8250	ns	26MIL
SPKR_N1_CONN	1	FTP4609	ns	26MIL

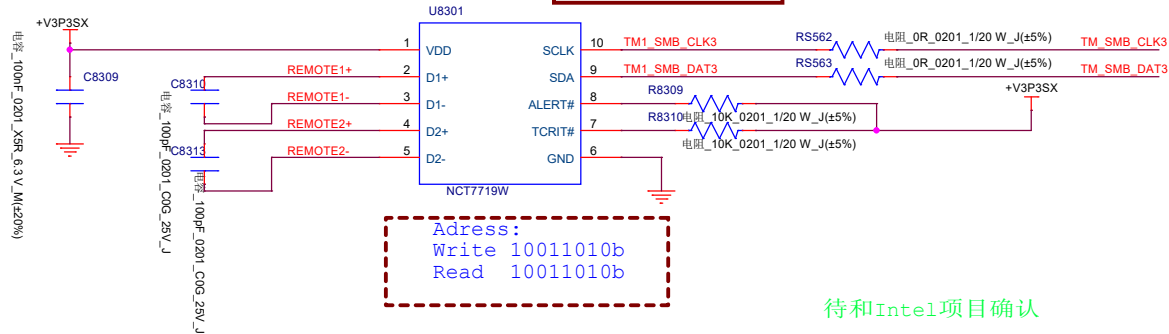
[illegible]

PCB trace width of SLEEVE &
RING2 are required at least 40
mil and its length should be
as short as possible.

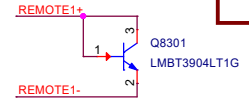
SLEEVE_CON_R	1	FTP8254	ns	26MIL
HPOL_CON	1	FTP8253	ns	26MIL
HPOR_CON	1	FTP8249	ns	26MIL
HPOUT_JD_CON	1	FTP8252	ns	26MIL
RING2_CON_R	1	FTP8251	ns	26MIL

REMOTE1+/-, Trace width/space:10/10 mil,Trace length:<8"
Connect guard traces to GND on either side of the
DXP-DXN traces

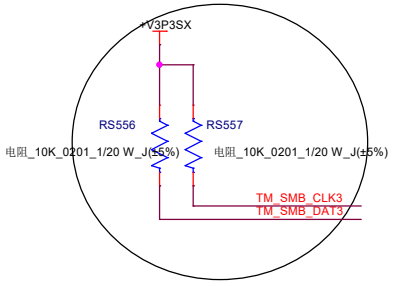
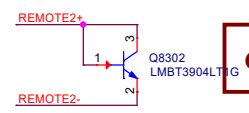
Charger Sensor



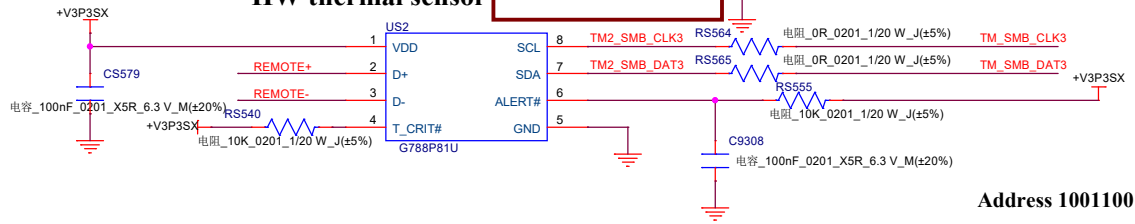
CPU Sensor



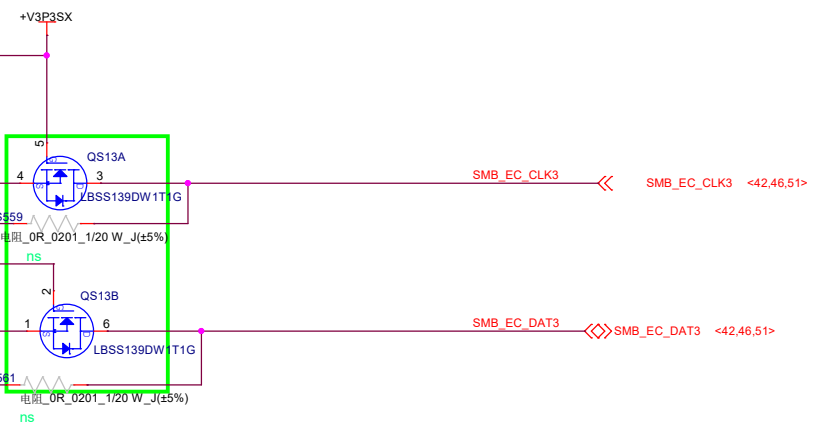
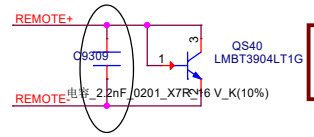
GPU Sensor

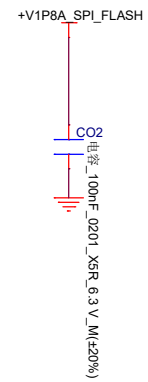
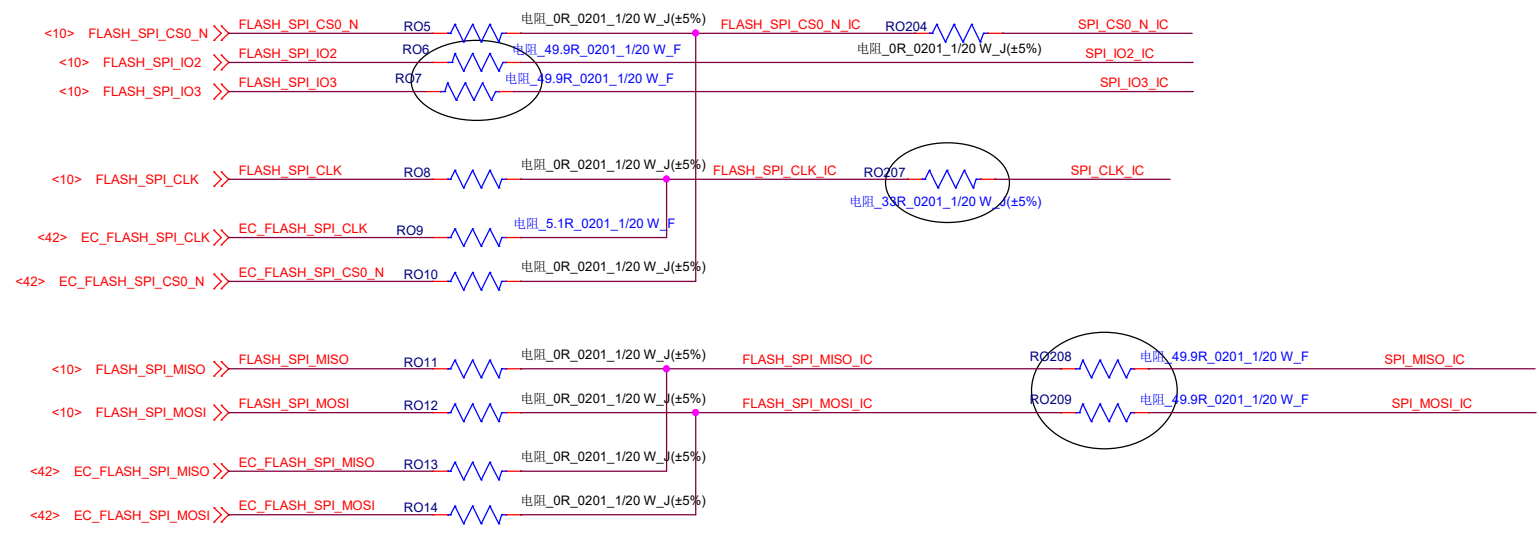
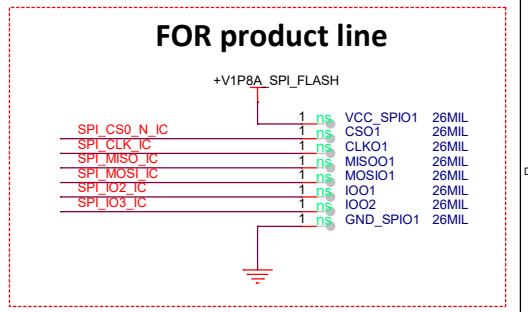
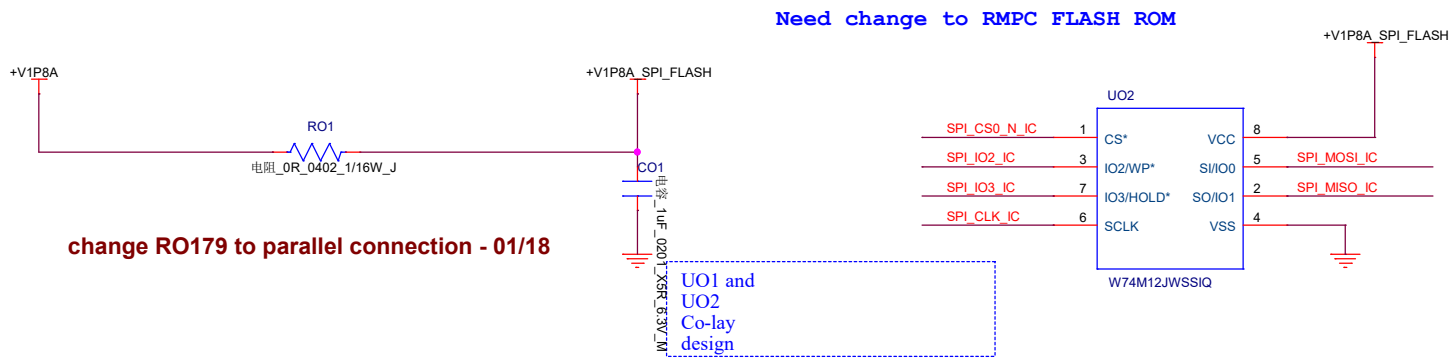


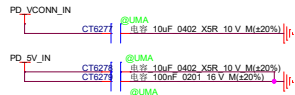
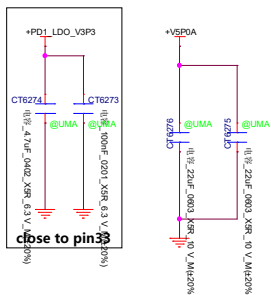
DDR Sensor



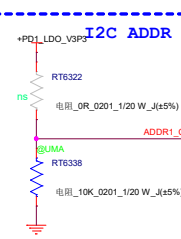
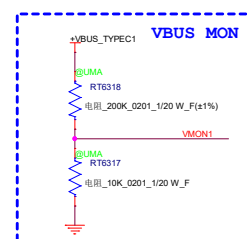
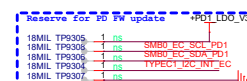
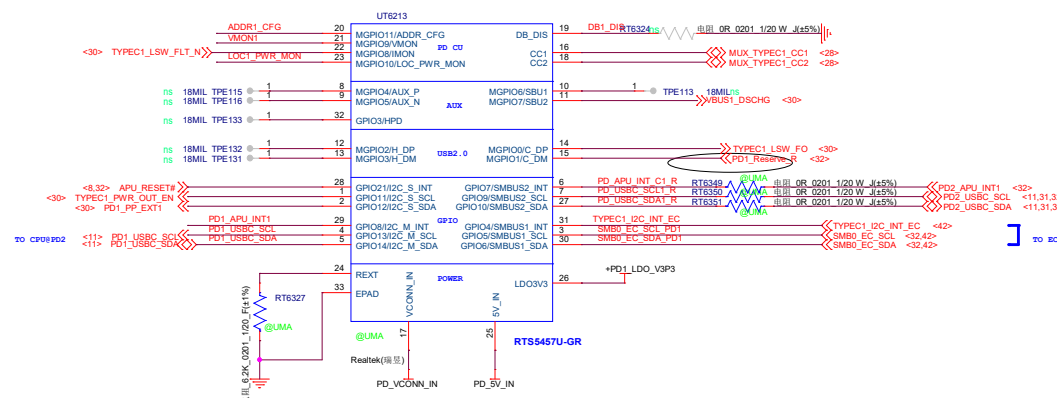
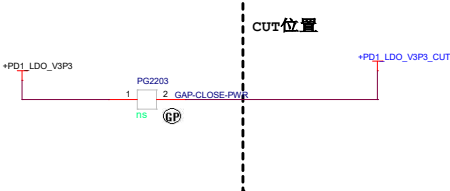
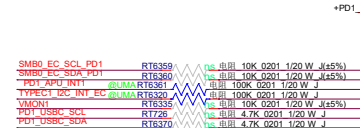
Environ Sensor



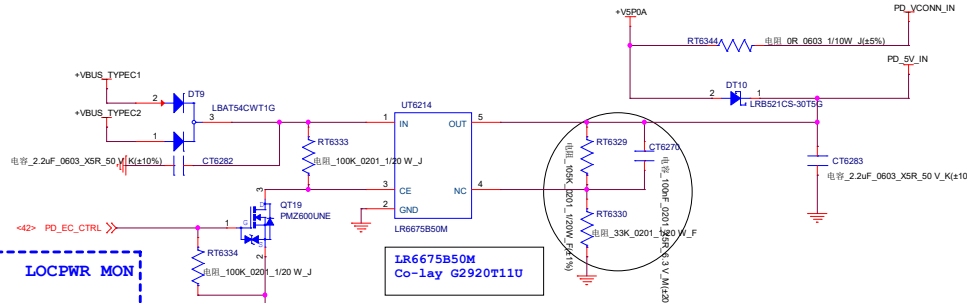
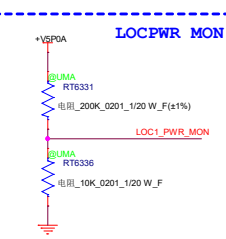


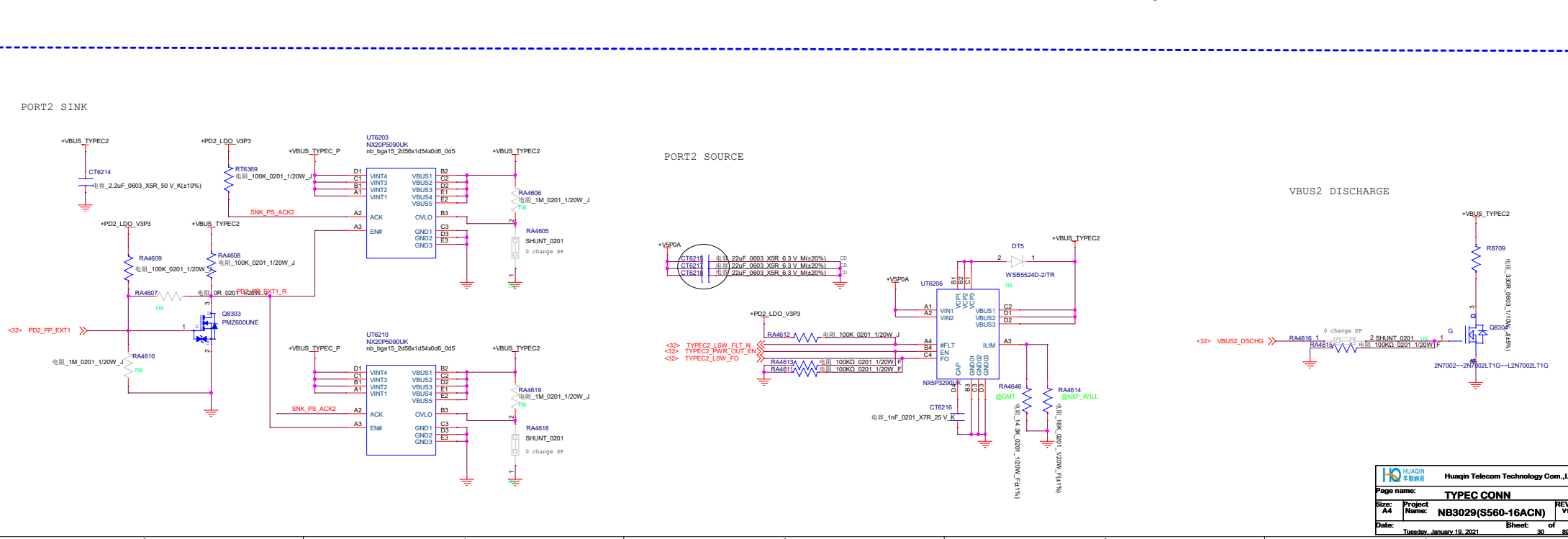
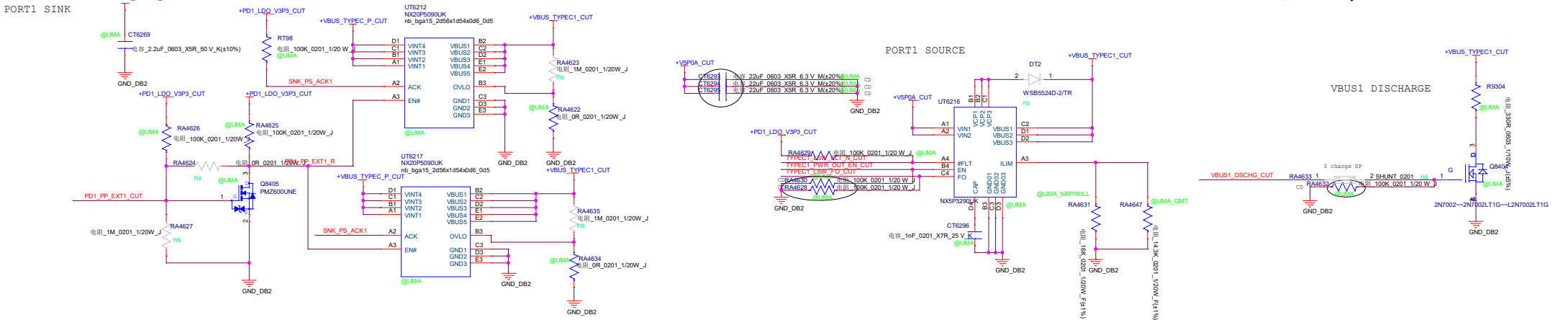
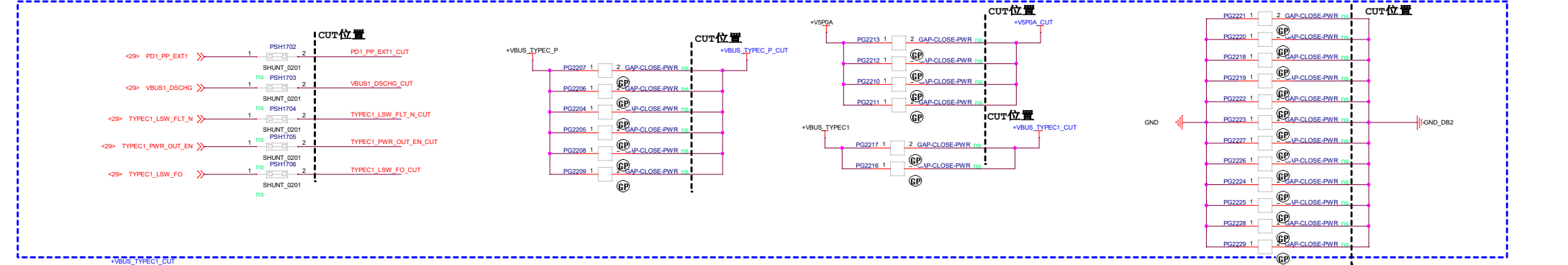


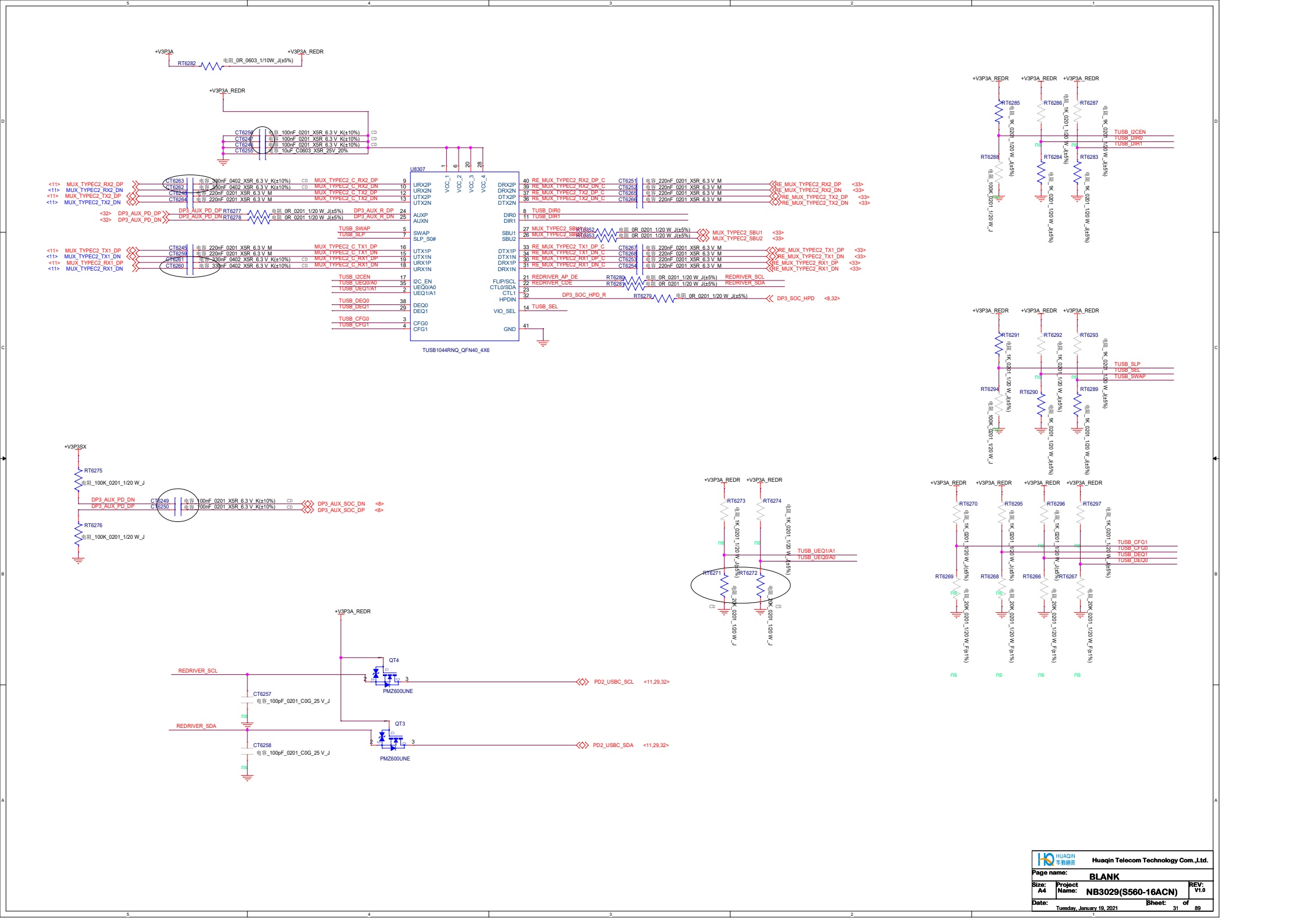
Slave Addr	Ra 5%	Rb 5%	
addr0:0xCC	NC	10K	<0.2V
addr1:0xCE	75K	10K	>=0.2V&&<0.6V
addr2:0xD0	33K	10K	>=0.6V&&<1.0V
addr3:0xD2	10K	10K	>=1.0V

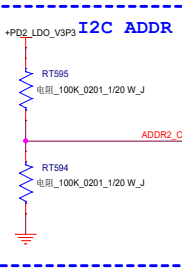
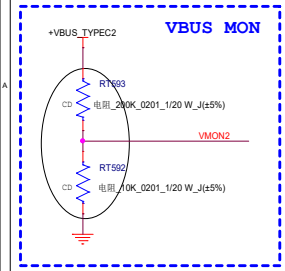
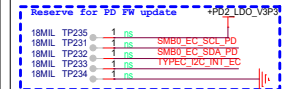
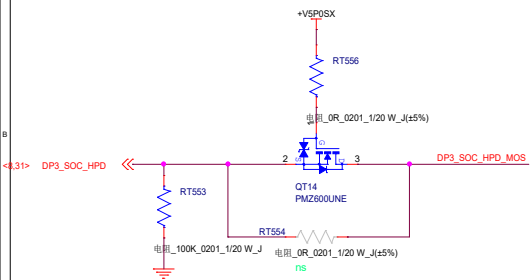
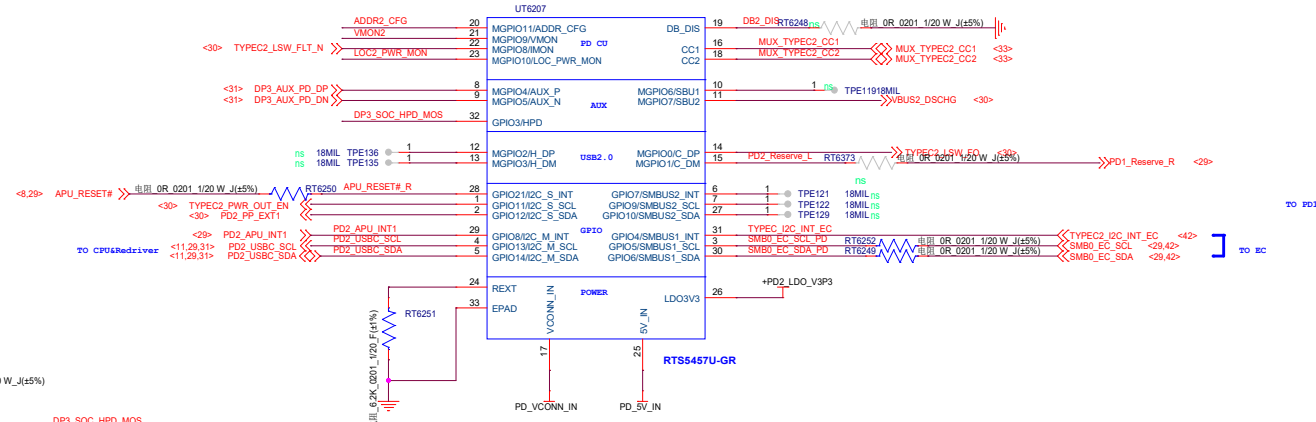
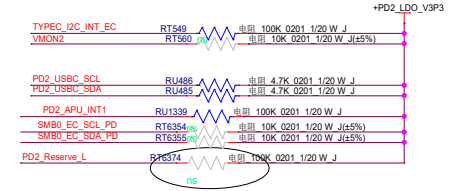
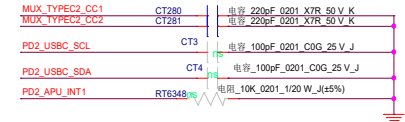
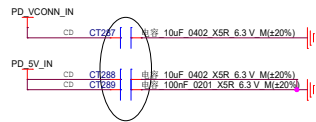
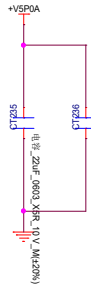
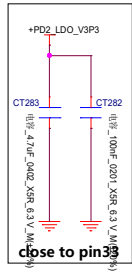


Slave Addr	Ra	Rb	
addr0:0xc4	NC	10K	<0.2V
addr1:0xc6	75K	10K	>=0.2V&&<0.6V
addr2:0xc8	33K	10K	>=0.6V&&<1.0V
addr3:0xca	10K	10K	>=1.0V

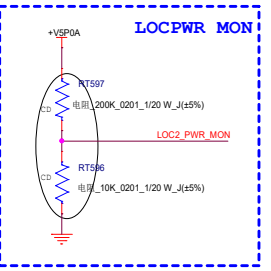


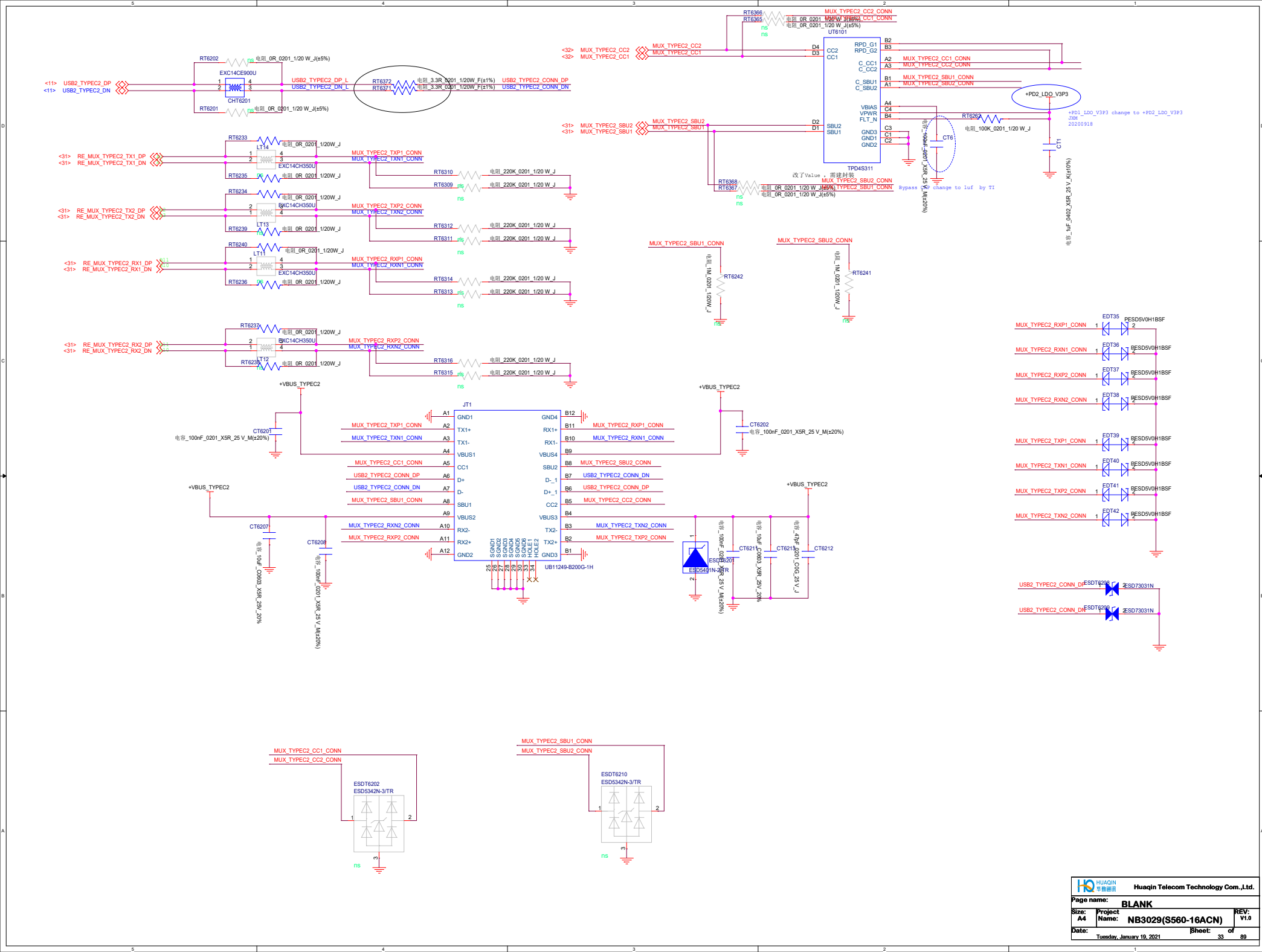




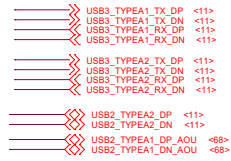


Slave Addr	Ra	Rb	
addr0:0xc4	NC	10K	<0.2V
addr1:0xc6	75K	10K	>=0.2V&&<0.6V
addr2:0xc8	33K	10K	>=0.6V&&<1.0V
addr3:0xca	10K	10K	>=1.0V

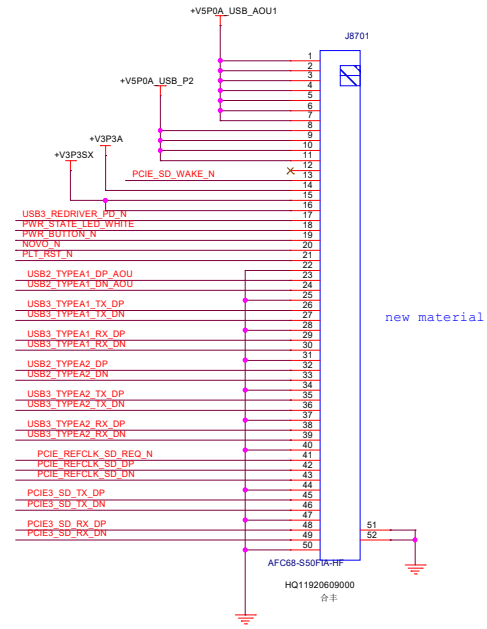
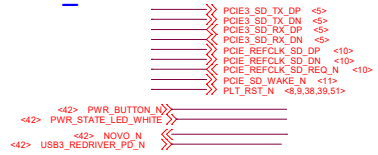




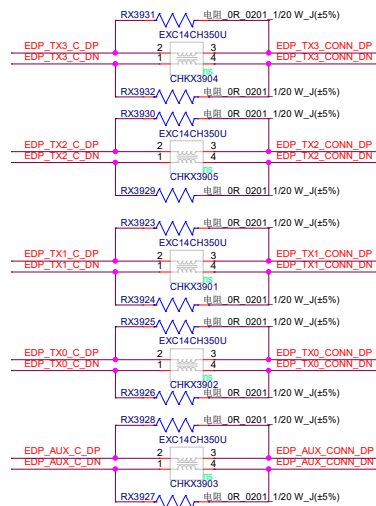
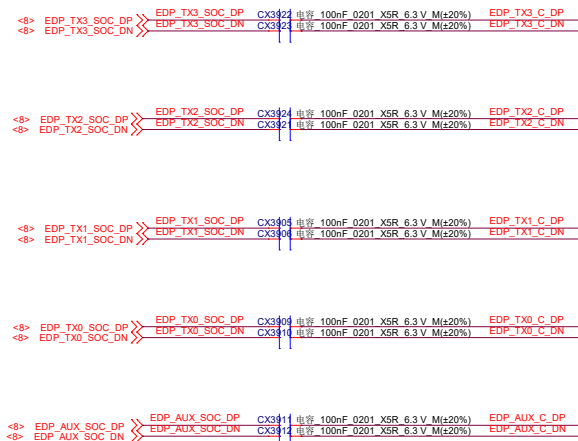
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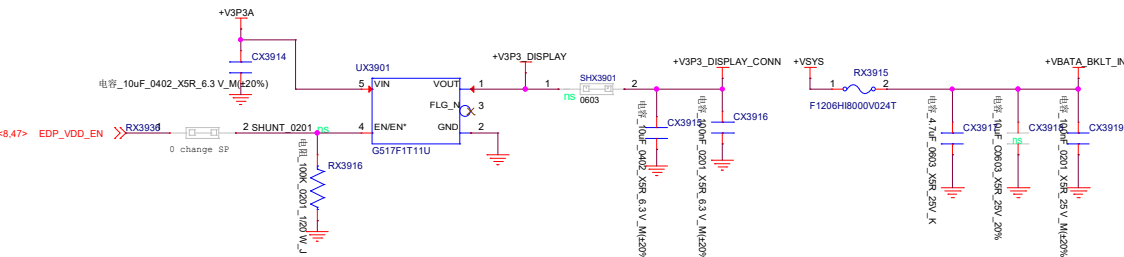
PCIE_SD



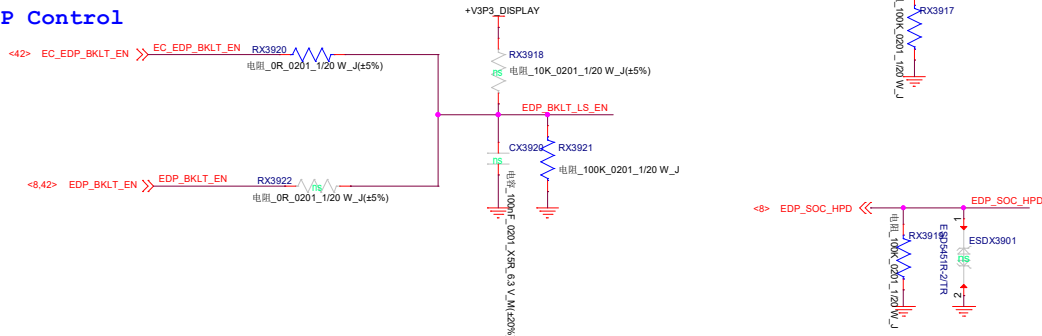
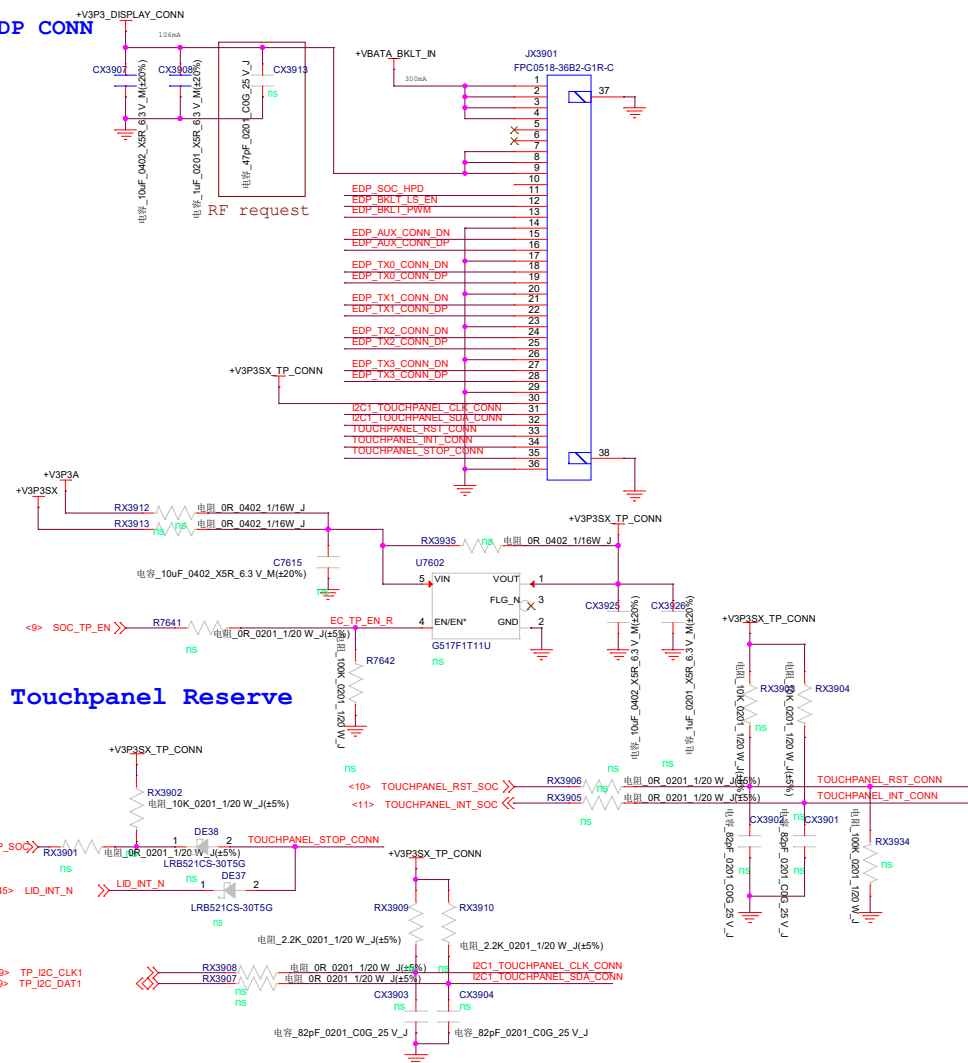
eDP Signal



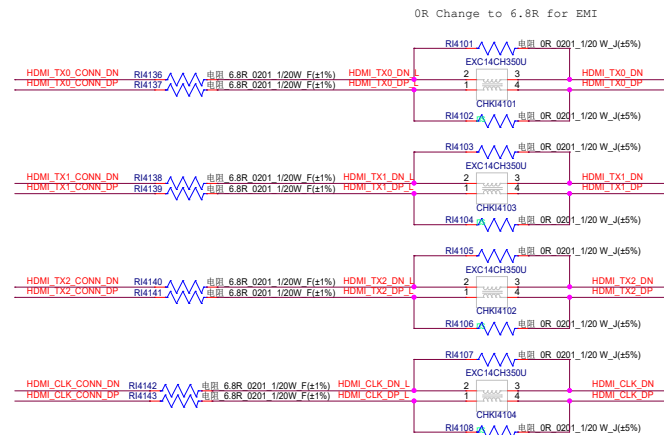
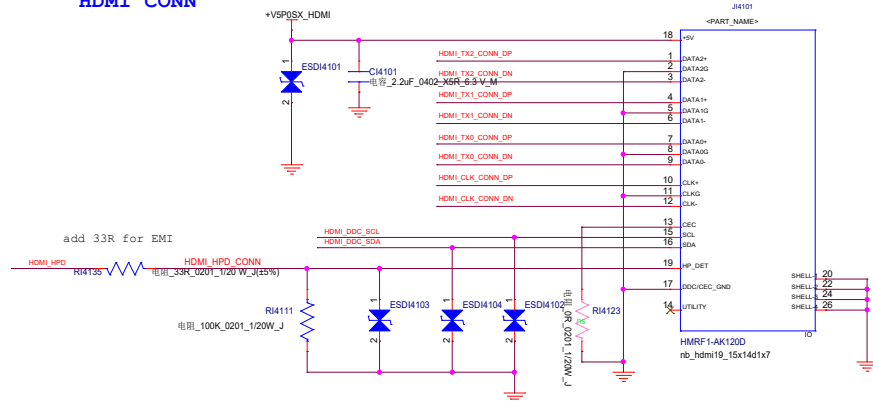
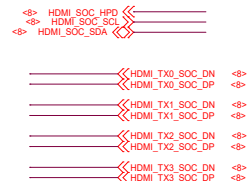
eDP VCC & BL Power



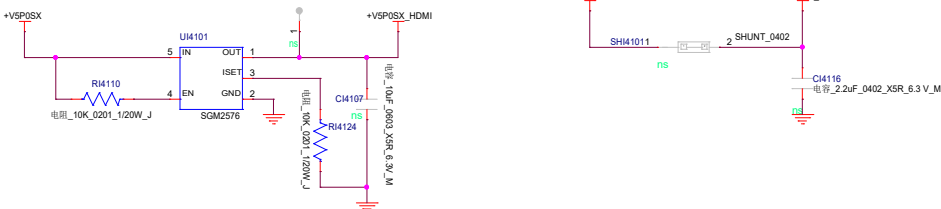
eDP Control

eDP CONN^{+V3}

HDMI CONN



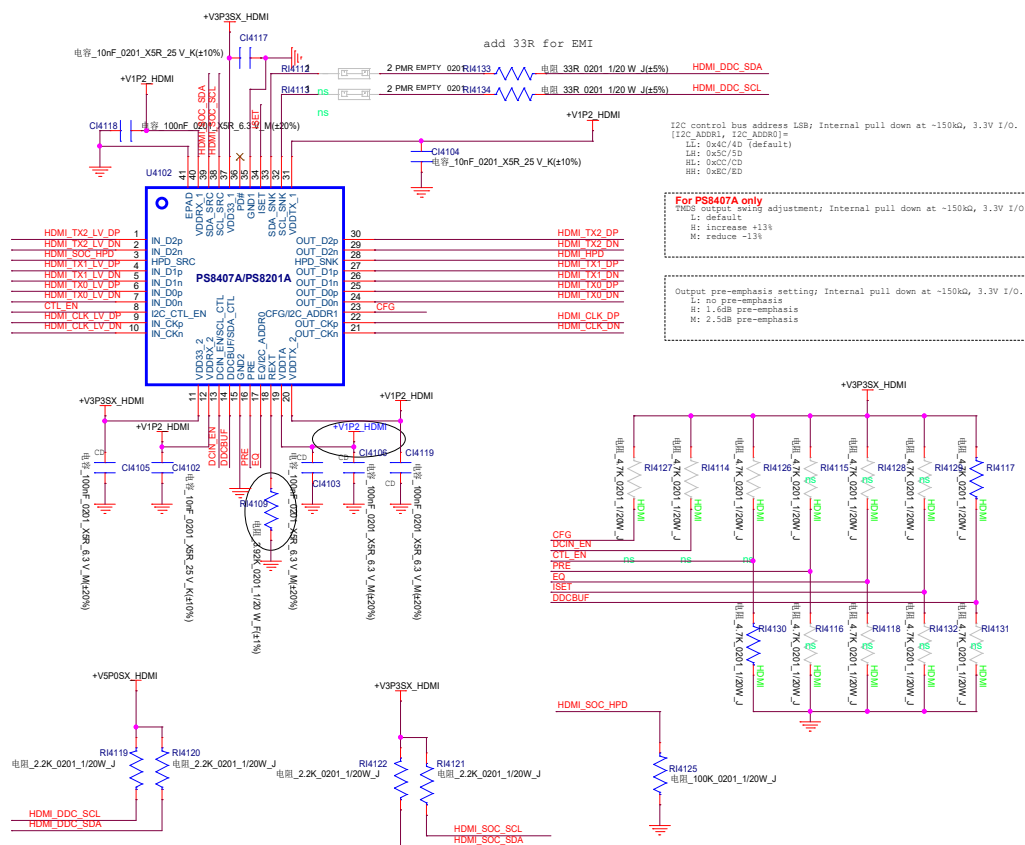
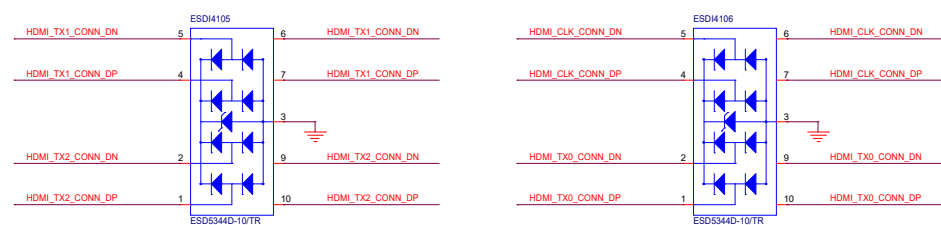
Power 1

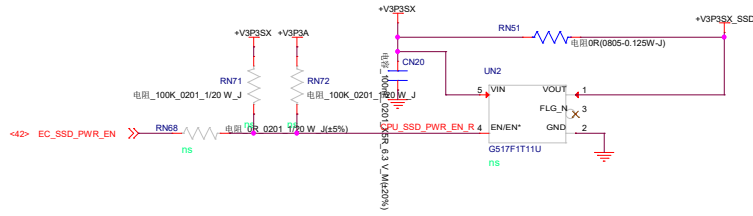


Signal

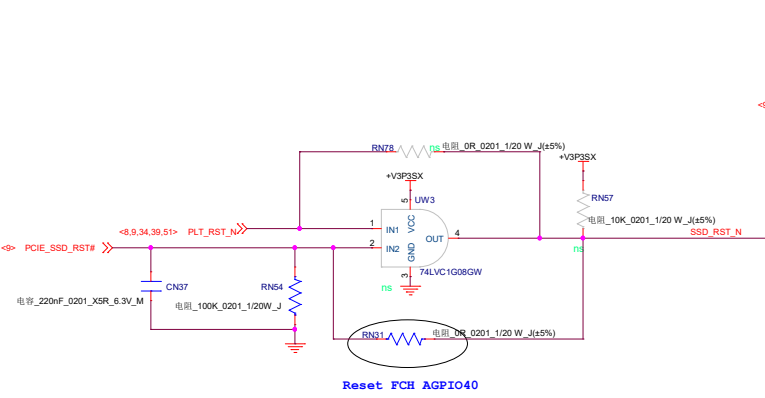
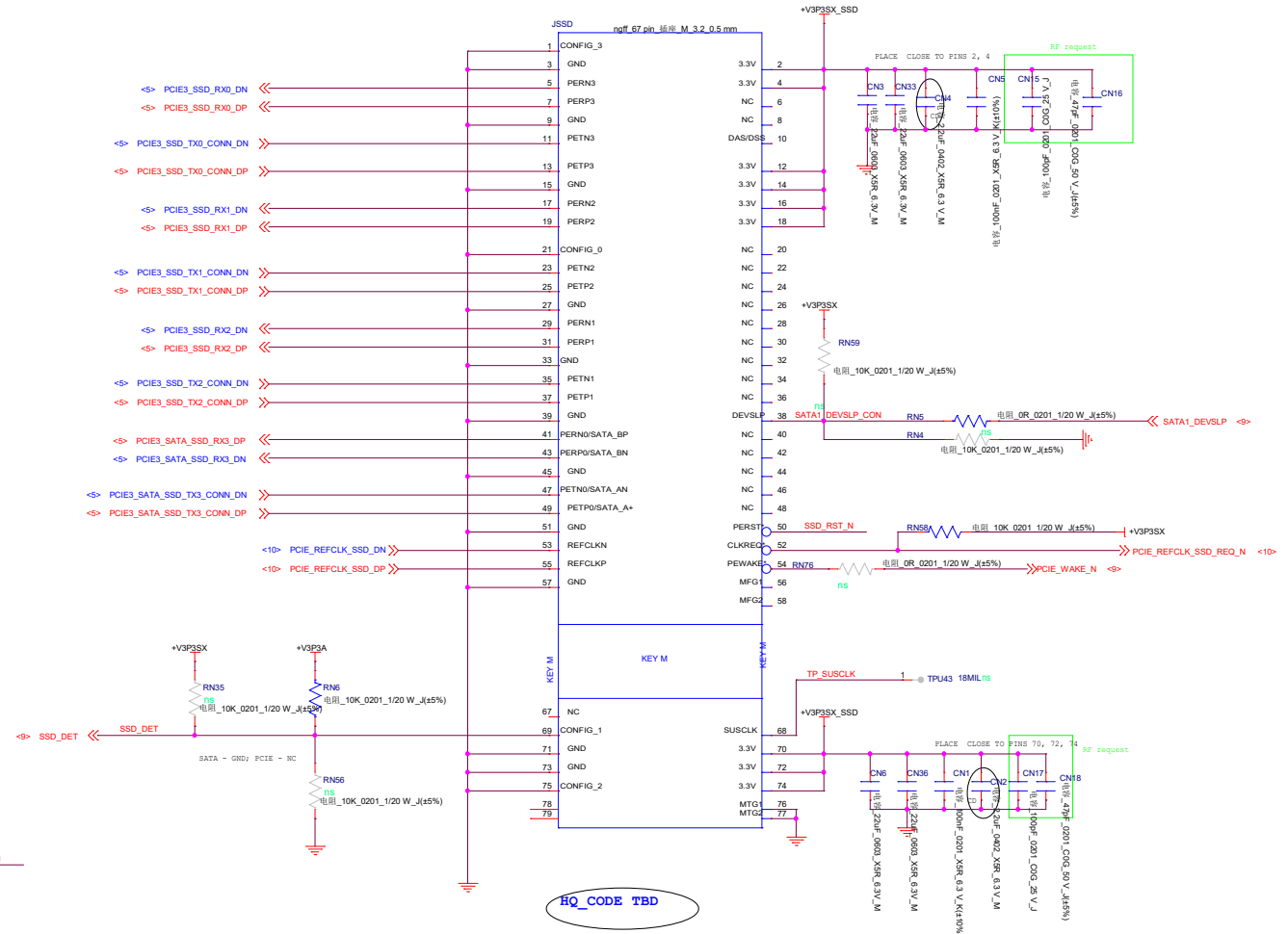
HDMI_TX2_LV_OD	CD_04108	直阻 100Ω 0201 XSR 6.3 V Min±20%	HDMI_TX0_SOC_OD
HDMI_TX2_LV_OD	CD_04109	直阻 100Ω 0201 XSR 6.3 V Min±20%	HDMI_TX0_SOC_OD
HDMI_TX1_LV_OD	CD_04110	直阻 100Ω 0201 XSR 6.3 V Min±20%	HDMI_TX1_SOC_OD
HDMI_TX1_LV_OD	CD_04111	直阻 100Ω 0201 XSR 6.3 V Min±20%	HDMI_TX1_SOC_OD
HDMI_TX0_LV_OD	CD_04112	直阻 100Ω 0201 XSR 6.3 V Min±20%	HDMI_TX2_SOC_OD
HDMI_TX0_LV_OD	CD_04113	直阻 100Ω 0201 XSR 6.3 V Min±20%	HDMI_TX2_SOC_OD
HDMI_CLK_LV_OD	CD_04114	直阻 100Ω 0201 XSR 6.3 V Min±20%	HDMI_TX3_SOC_OD
HDMI_CLK_LV_OD	CD_04115	直阻 100Ω 0201 XSR 6.3 V Min±20%	HDMI_TX3_SOC_OD

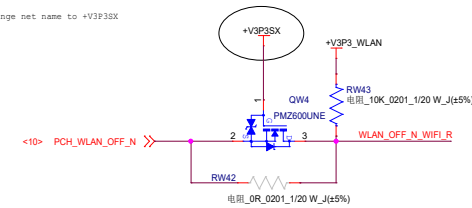
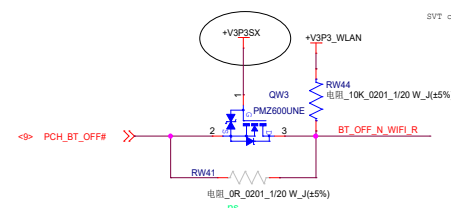
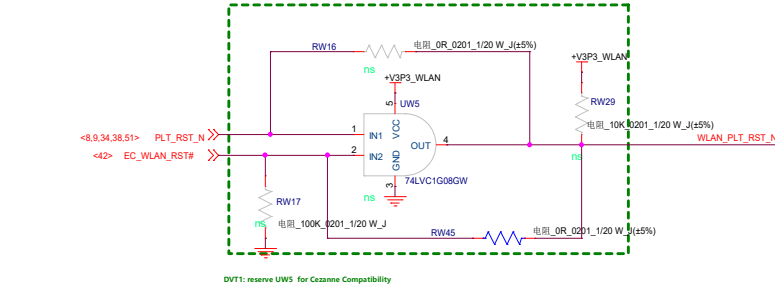
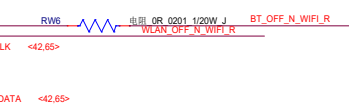
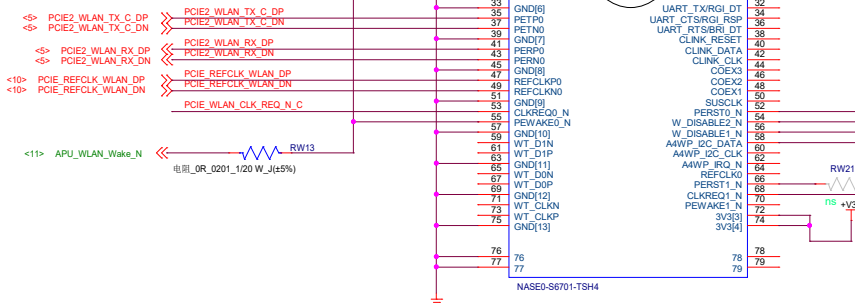
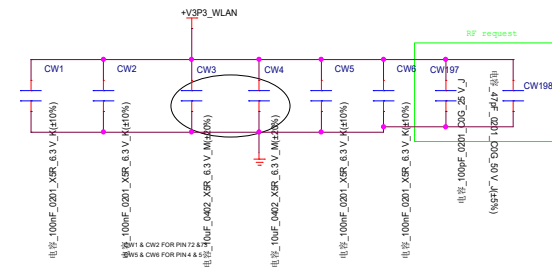
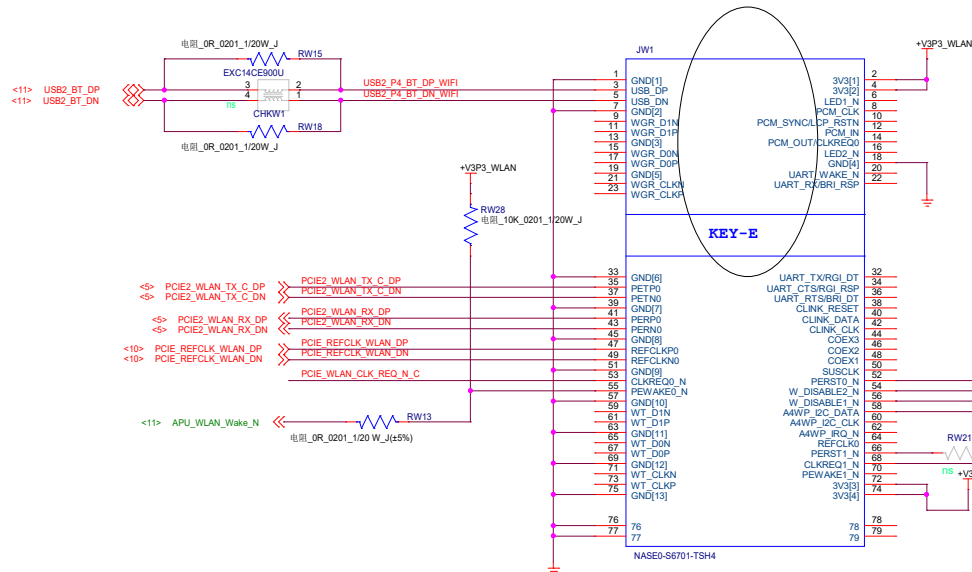
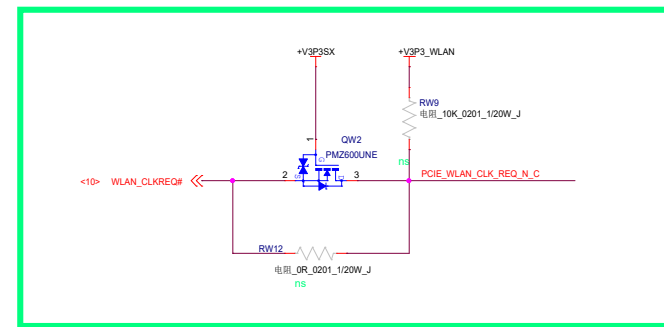
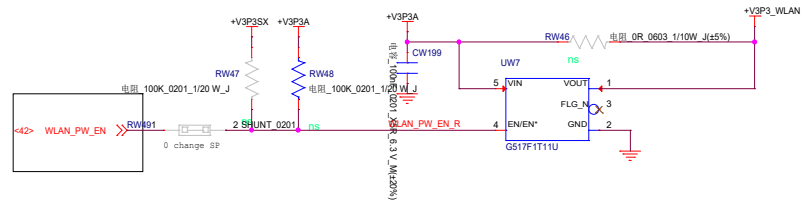
ESD





SSD

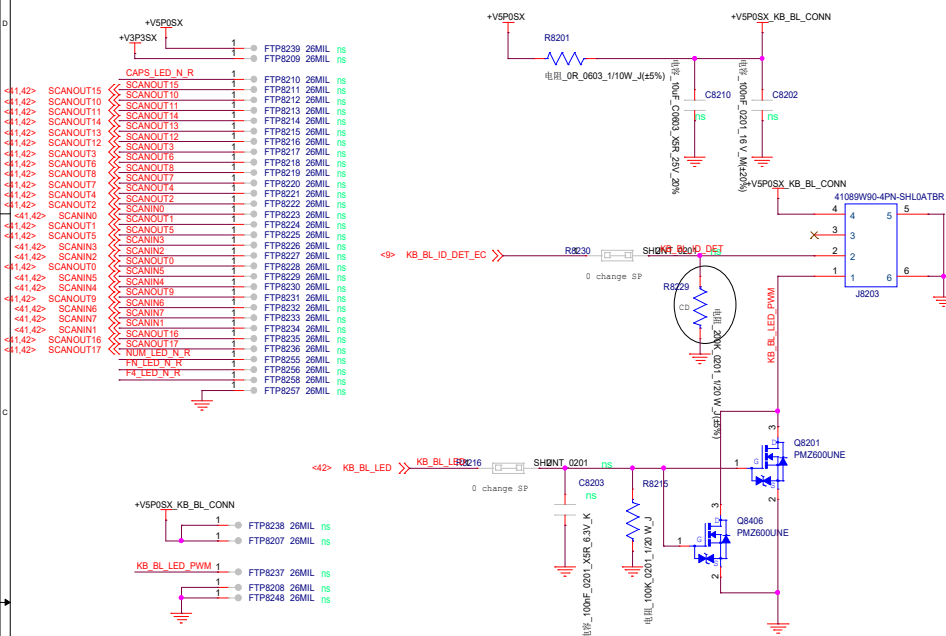




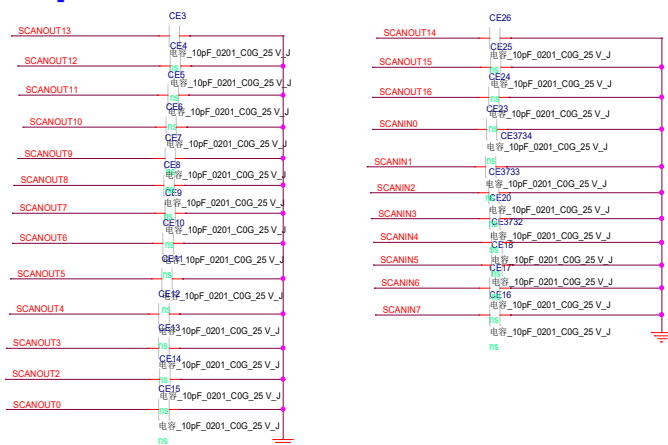
DVT1: reserve UW5 for Cezanne Compatibility

	5	4	3	2	1
D					
C					
B					
A					

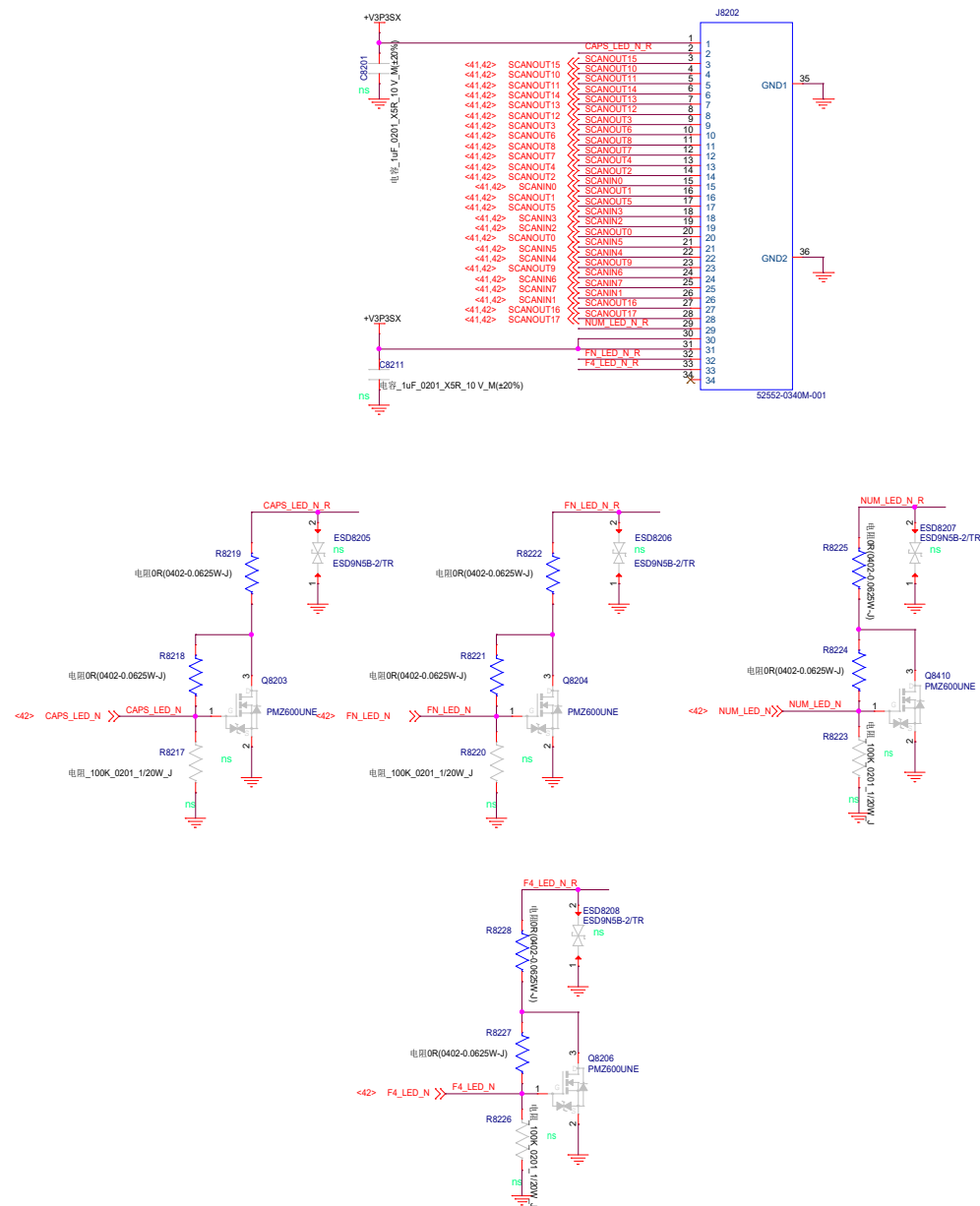
KB Backlight



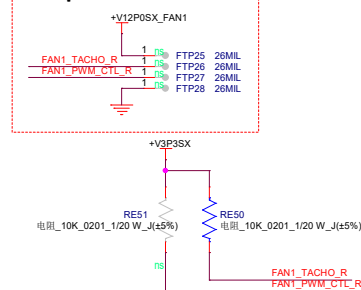
EMC Require Reserved



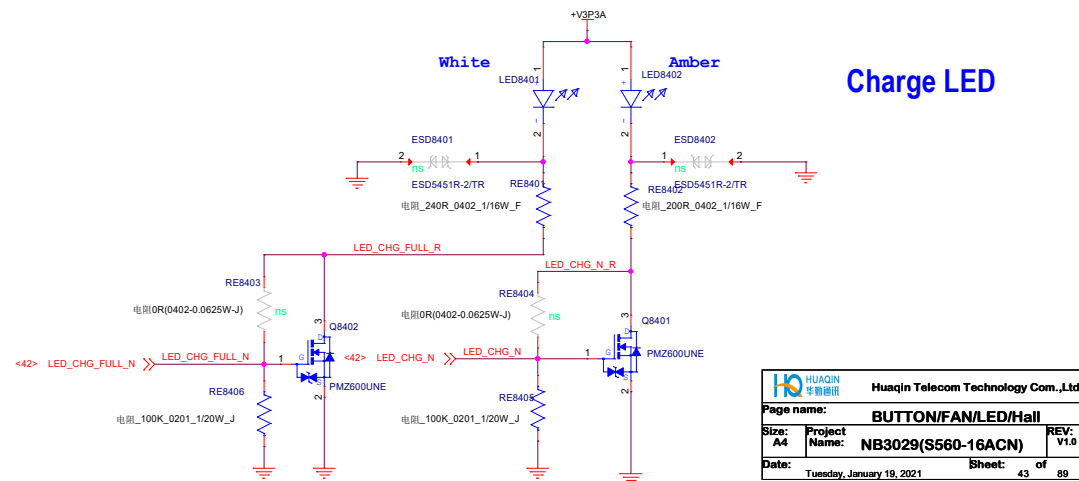
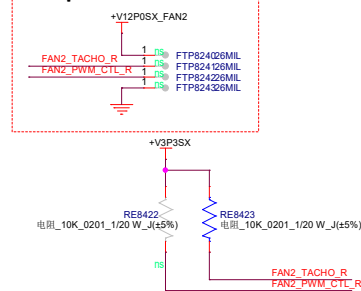
KB CONN




FOR product line

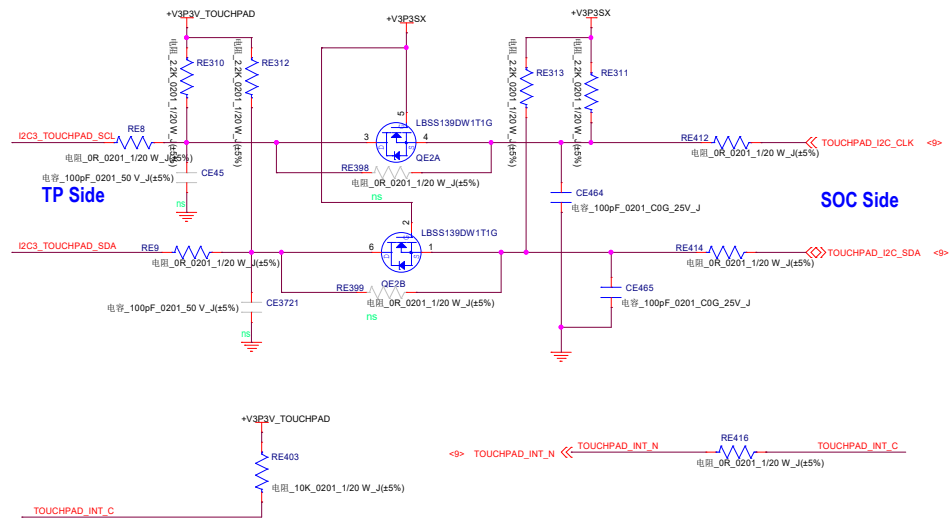


FOR product line

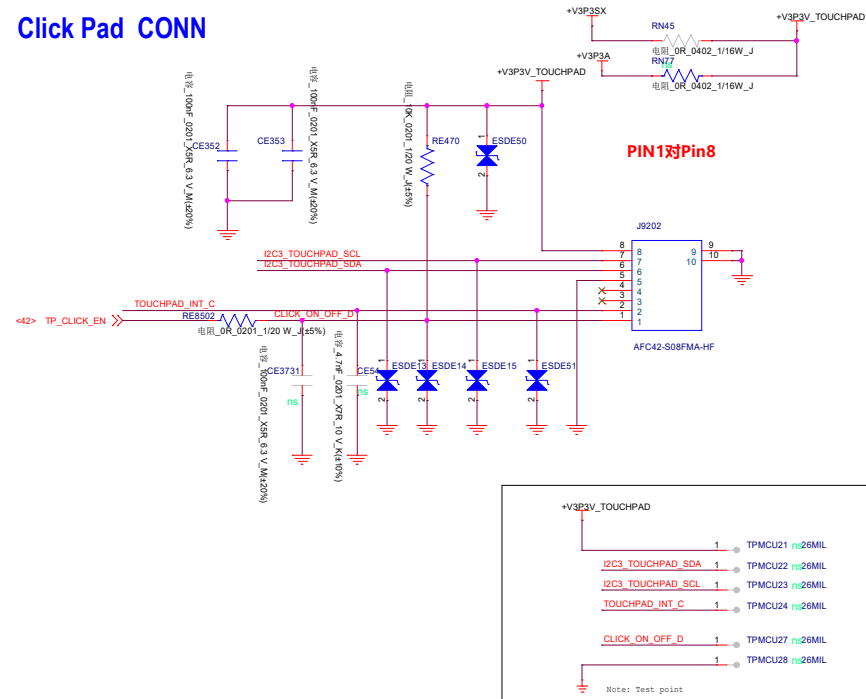


 HUAQIN 华勤通讯		Huaqin Telecom Technology Com.,Ltd.	
Page name:		BUTTON/FAN/LED/Hall	
Size: A4	Project Name: NB3029(S560-16ACN)	REV: V1.0	
Date: Tuesday, January 19, 2021	Sheet:	43	of 89

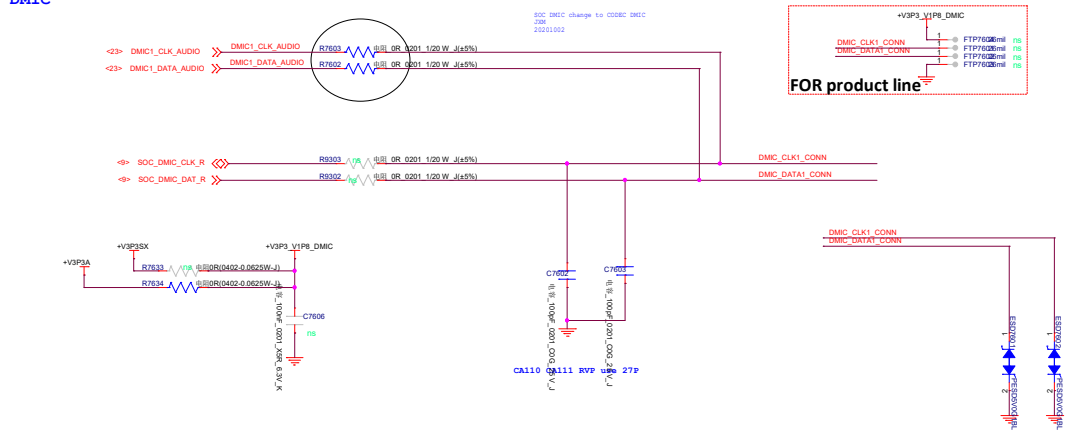
Touch Pad



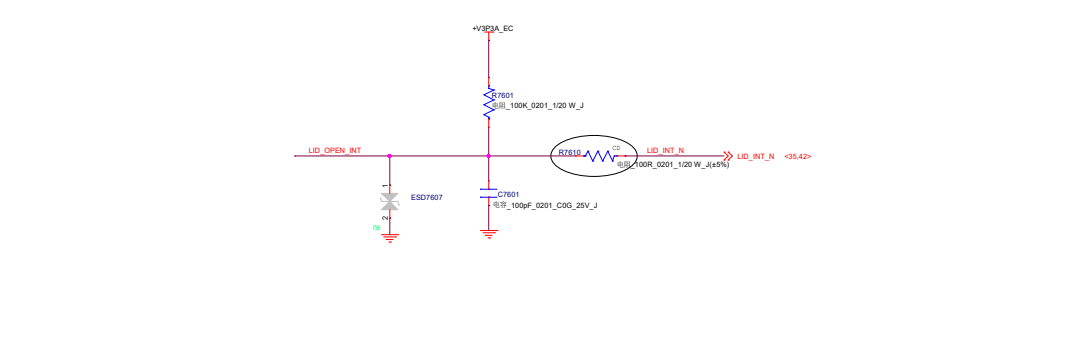
Click Pad CONN



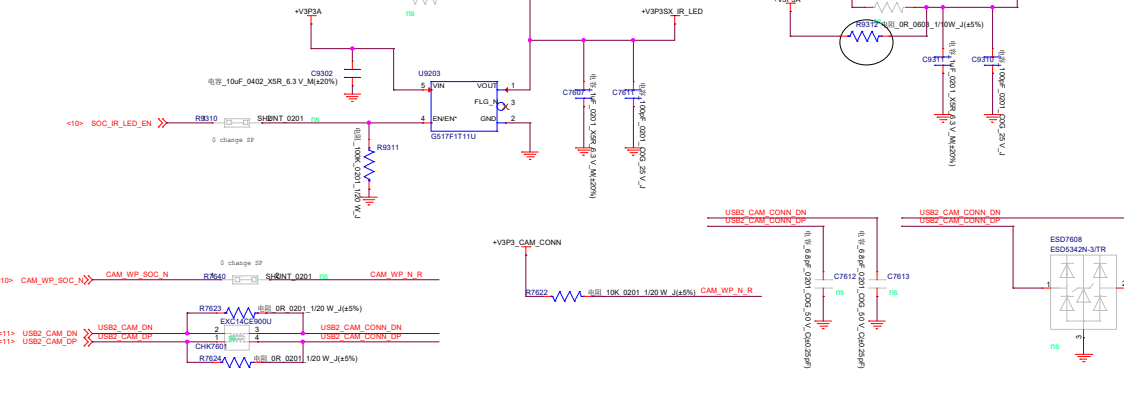
DMIC



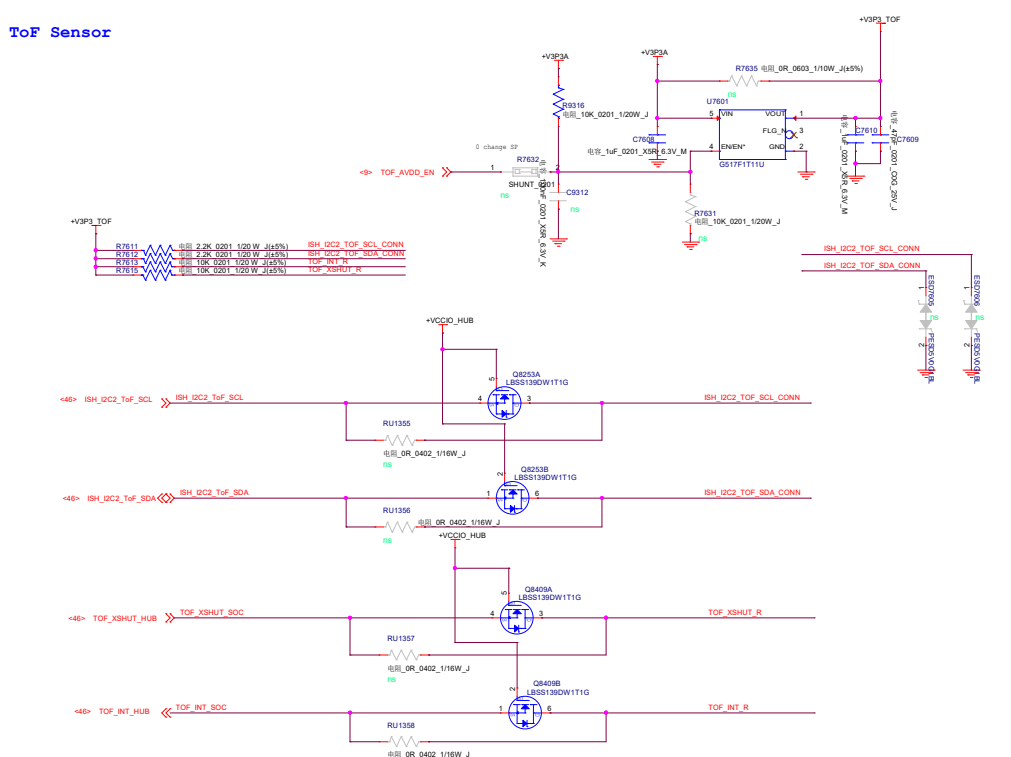
Hall Sensor



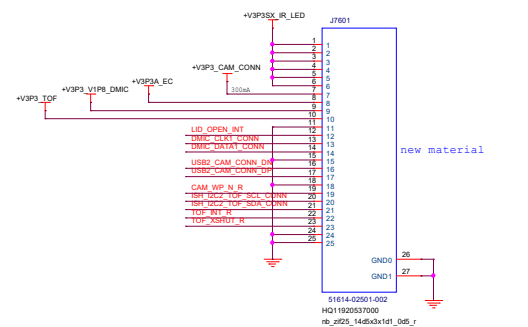
Camera



ToF Sensor

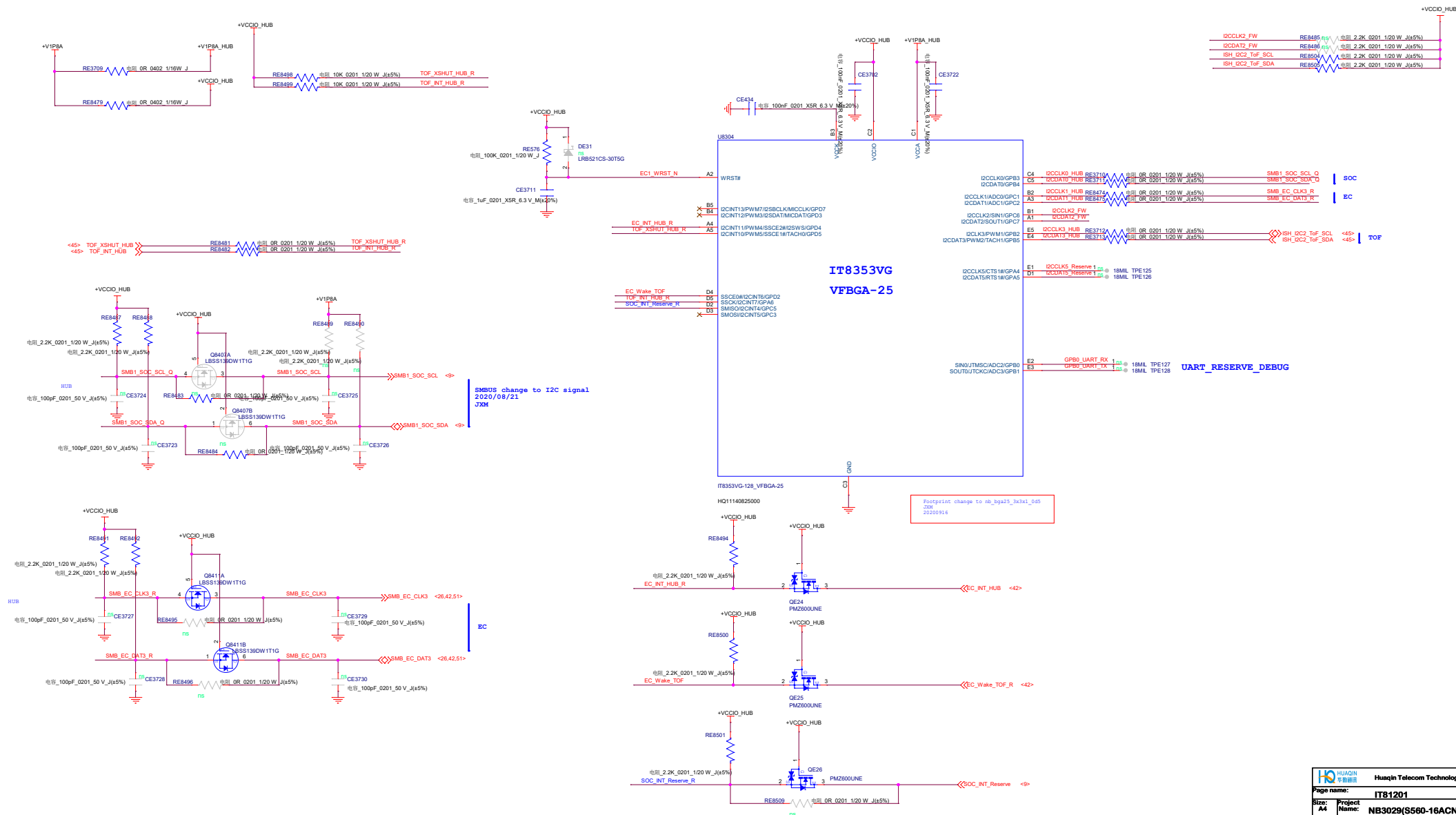


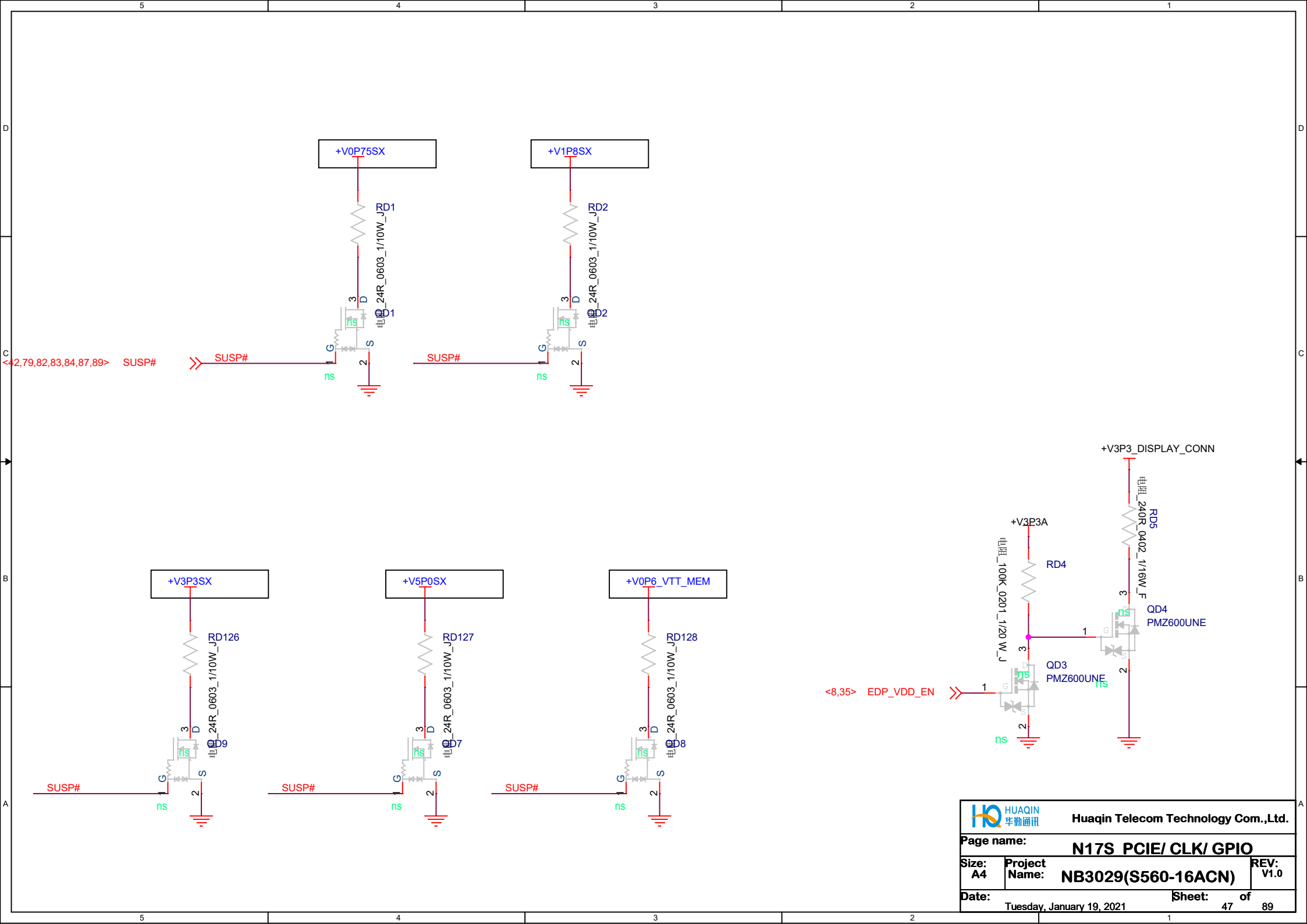
TOE/ IB CAM/ DMIC/ AIS CONN

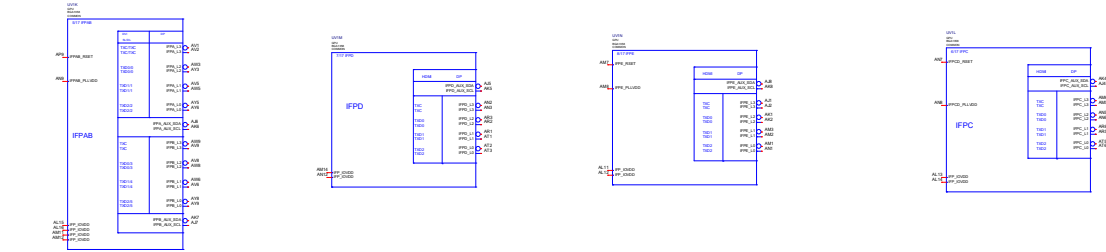


Note: TY2 nb con30 19d2x5d2x1d95 0d5 Bin1 right



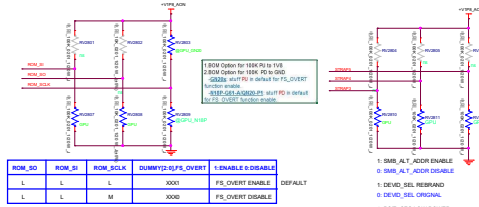






IFP

SPI&STRAP



STRAP0	STRAP1	STRAP2	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
M	H	H	0	1	1	1
M	H	L	0	1	1	0
M	L	H	0	1	0	1
M	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

DEFAULT

GPIO	IO	FUNCTION	RAMCFG0	STRAP0	STRAP1	STRAP2
GPIO0	OUT	PWM Output to control NVDD	0 (0x0000)	L	L	L
GPIO1	OUT	FB Enable for GC2.1	1 (0x0001)	L	L	L
GPIO2	IN	GPU wake signal for GC2.1	0 (0x0000)	L	L	L
GPIO3	OUT	PWM Output to control the SRAM power supply	1 (0x0001)	L	L	L
GPIO4	OUT	GPU power sequencing for GC2.1.1 - 1V8_MAIN_EN	2 (0x0002)	L	L	L
GPIO5	IN	Active low Frame Lock	0 (0x0000)	L	L	L
GPIO6	OUT	Phase Shredding NVDD_PSI	0 (0x0000)	L	L	L
GPIO7	OUT	Panel Backlight enable	0 (0x0000)	L	L	L
GPIO8	OUT	Memory voltage control	0 (0x0000)	L	L	L
GPIO9	IO	Active Low Thermal Alert	0 (0x0000)	L	L	L
GPIO10	OUT	Memory VREF Control (100K pull down)	0 (0x0000)	L	L	L
GPIO11	OUT	Panel Power enable	0 (0x0000)	L	L	L
GPIO12	IN	AC power detect or power supply overvoltage input (10K pull high)	0 (0x0000)	L	L	L
GPIO13	OUT	LCD Panel Backlight Enable	0 (0x0000)	L	L	L
GPIO14	IN	Hot Plug Detect for IFPA	0 (0x0000)	L	L	L
GPIO15	IN	Hot Plug Detect for IFPB	0 (0x0000)	L	L	L
GPIO16	OUT	System side PCIe reset monitor	0 (0x0000)	L	L	L
GPIO17	IN	Hot Plug Detect for IFPD	0 (0x0000)	L	L	L
GPIO18	IN	Hot Plug Detect for IFPE	0 (0x0000)	L	L	L
GPIO19	OUT	SD Vision LRM Signal	0 (0x0000)	L	L	L
GPIO20	NA	GC2.1_WAKE	0 (0x0000)	L	L	L
GPIO21	IO	UNUSED	0 (0x0000)	L	L	L
GPIO22	IO	UNUSED	0 (0x0000)	L	L	L
GPIO23	OUT	GPU PCIe self-reset control	0 (0x0000)	L	L	L
GPIO24	IN	Hot Plug Detect for IFPF	0 (0x0000)	L	L	L
GPIO25	NA	UNUSED	0 (0x0000)	L	L	L
GPIO26	NA	UNUSED	0 (0x0000)	L	L	L
GPIO27	IN	Hot Plug Detect for IFPC	0 (0x0000)	L	L	L

N18P-G0 GPIO (Update later)

GPIO	IO	ACTIVE	Function Description	IO Termination
GPIO0	OUT	-	PWM Output to control NVDD	
GPIO1	OUT	-	FB Enable for GC2.1	
GPIO2	IN	-	GPU wake signal for GC2.1	
GPIO3	OUT	-	PWM Output to control the SRAM power supply	
GPIO4	OUT	-	GPU power sequencing for GC2.1.1 - 1V8_MAIN_EN	
GPIO5	IN	NA	Active low Frame Lock	
GPIO6	OUT	-	Phase Shredding NVDD_PSI	
GPIO7	OUT	NA	Panel Backlight enable	
GPIO8	OUT	-	Memory voltage control	
GPIO9	IO	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control (100K pull down)	
GPIO11	OUT	-	Panel Power enable	
GPIO12	IN	-	AC power detect or power supply overvoltage input (10K pull high)	
GPIO13	OUT	NA	LCD Panel Backlight Enable	
GPIO14	IN	NA	Hot Plug Detect for IFPA	
GPIO15	IN	NA	Hot Plug Detect for IFPB	
GPIO16	OUT	-	System side PCIe reset monitor	
GPIO17	IN	NA	Hot Plug Detect for IFPD	
GPIO18	IN	NA	Hot Plug Detect for IFPE	
GPIO19	OUT	NA	SD Vision LRM Signal	
GPIO20	NA	GC2.1_WAKE		
GPIO21	IO	UNUSED		
GPIO22	IO	UNUSED		
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24	IN	NA	Hot Plug Detect for IFPF	
GPIO25	NA	UNUSED		
GPIO26	NA	UNUSED		
GPIO27	IN	NA	Hot Plug Detect for IFPC	

STRAP0	STRAP1	STRAP2	RAMCFG0
L	L	L	0000
L	H	L	0010
L	H	H	0011
H	H	L	0010
H	H	H	0011

ROM_ID	ROM_SI	ROM_SCLK	DUMWYD-S/P_S_OVERT	1-ENABLE 0-DISABLE
L	L	L	XXXX	PS_OVERT ENABLE
L	L	M	XXXX	PS_OVERT DISABLE

STRAP0	STRAP1	STRAP2	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

High / Test to 1.8V
Mid-Mid / Test to 0.9V
Low / Test to 0V

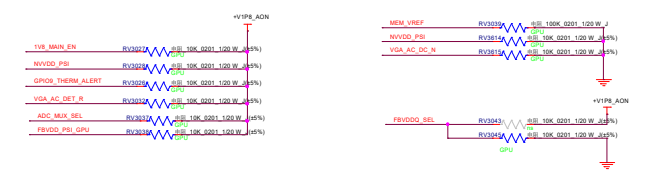
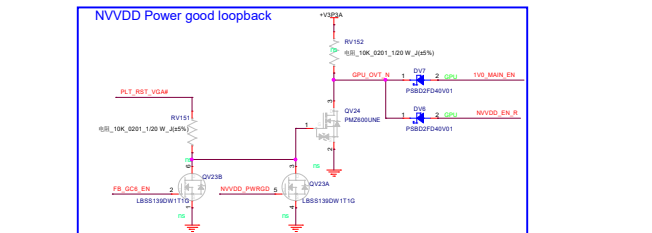
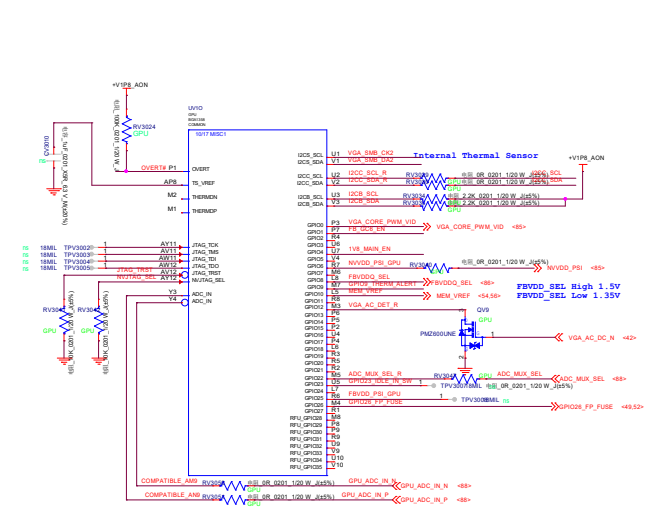
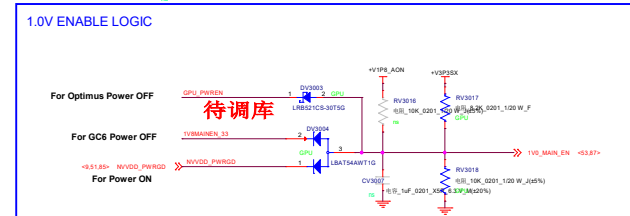
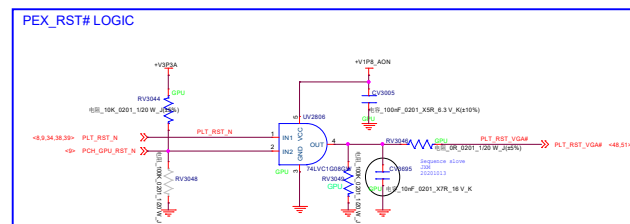
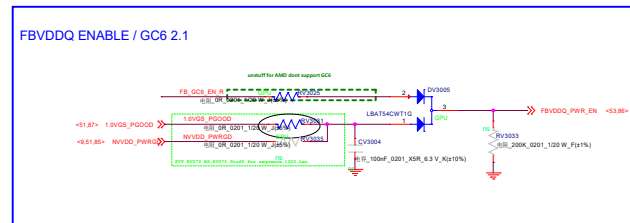
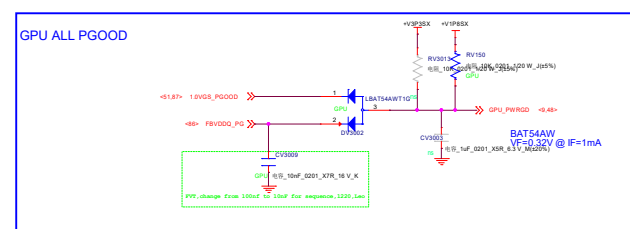
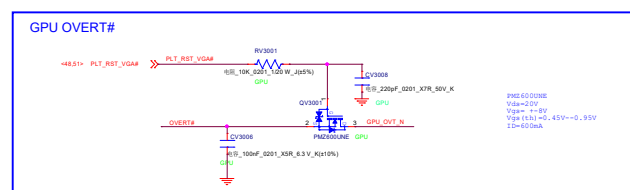
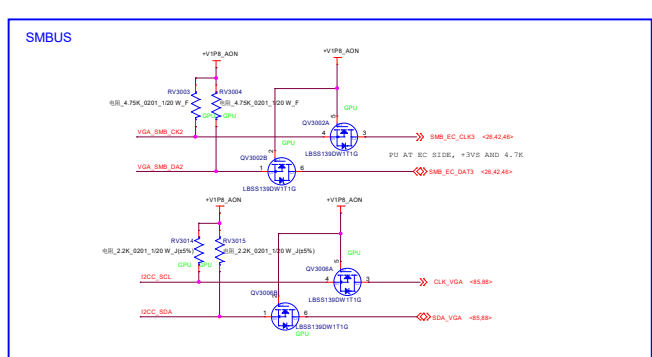
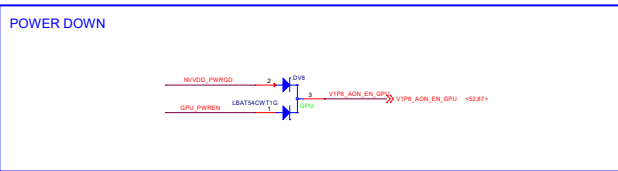
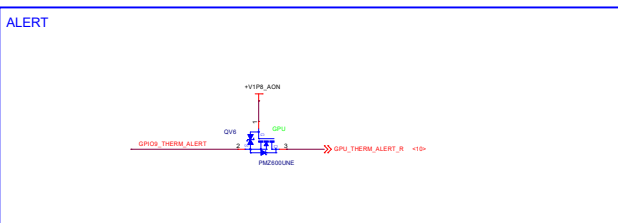
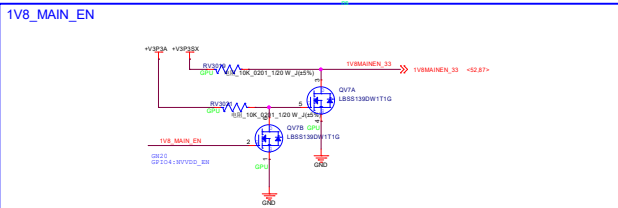
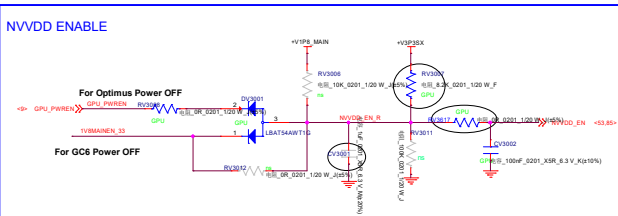
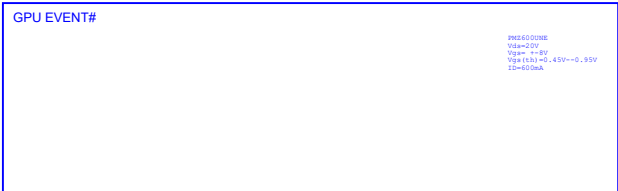
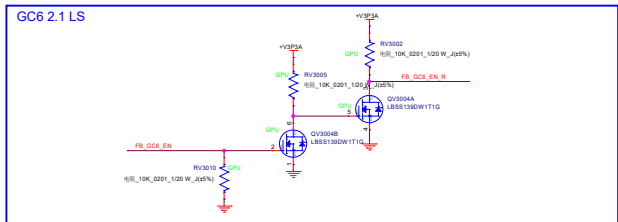
1-SMB_ALT_ADDR ENABLE
0-SMB_ALT_ADDR DISABLE
1-DEVID_SEL REBRAND
0-DEVID_SEL ORIGINAL
1-PCIE_CFG LOW POWER
0-PCIE_CFG HIGH POWER
1-VGA_DEVICE ENABLE
0-VGA_DEVICE DISABLE

Default

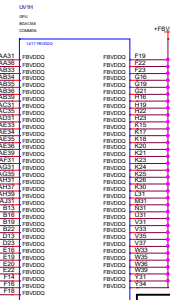
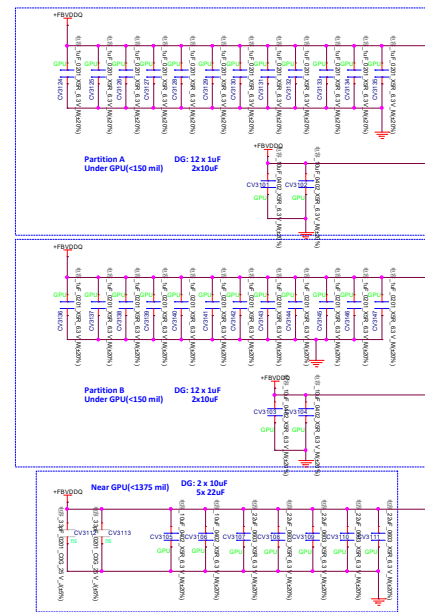
N18P-G0 Max-Q Power Sequence (Update later)



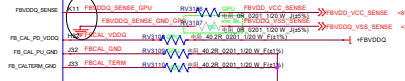
1. P11 power and P12 power are low, and P13 power is high.
2. P11 power and P12 power are high, and P13 power is low.
3. P11 power and P12 power are high, and P13 power is high.
4. P11 power and P12 power are low, and P13 power is high.
5. P11 power and P12 power are low, and P13 power is low.
6. P11 power and P12 power are high, and P13 power is low.
7. P11 power and P12 power are high, and P13 power is high.
8. P11 power and P12 power are low, and P13 power is high.
9. P11 power and P12 power are low, and P13 power is low.
10. P11 power and P12 power are high, and P13 power is low.
11. P11 power and P12 power are high, and P13 power is high.
12. P11 power and P12 power are low, and P13 power is high.
13. P11 power and P12 power are low, and P13 power is low.
14. P11 power and P12 power are high, and P13 power is low.
15. P11 power and P12 power are high, and P13 power is high.



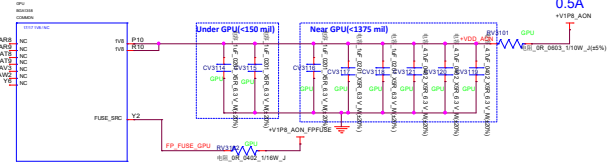
5A Peak 8A



CALIBRATION PIN	GDDR5
FB CAL x PD VDDQ	40.20ohm
FB CAL x PU GND	40.20ohm
FB CAL xTERM GND	40.20ohm

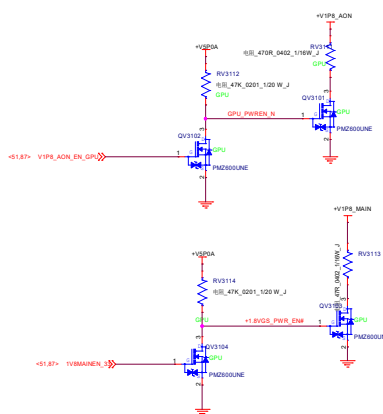
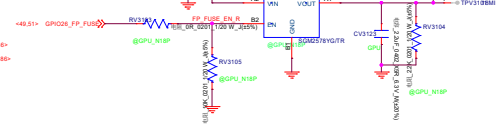


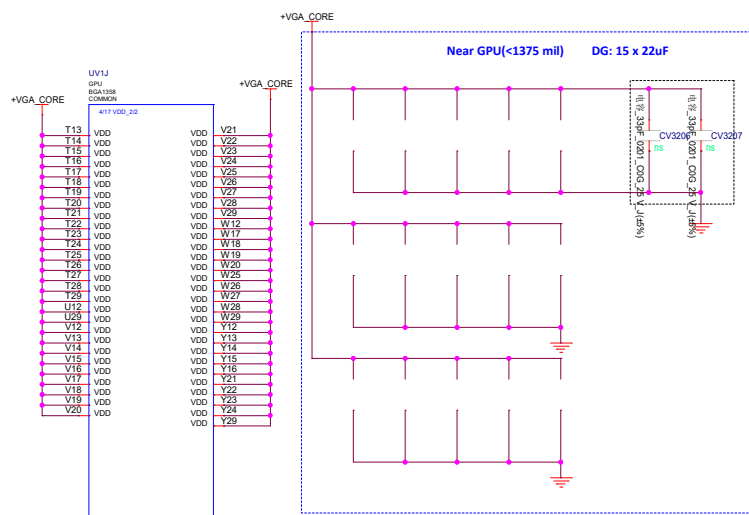
1.8V Total 1A (AON+MAIN)



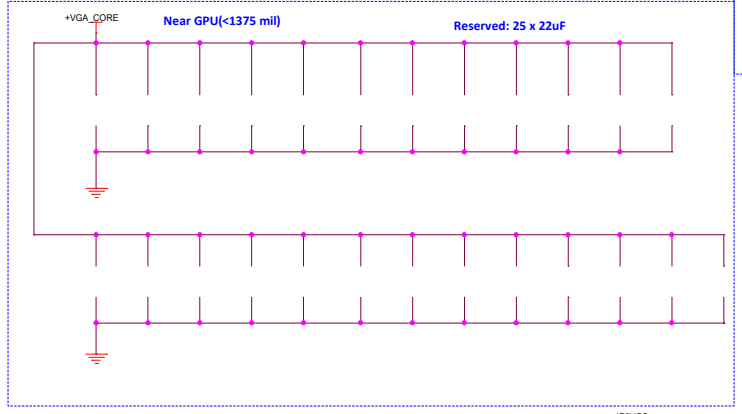
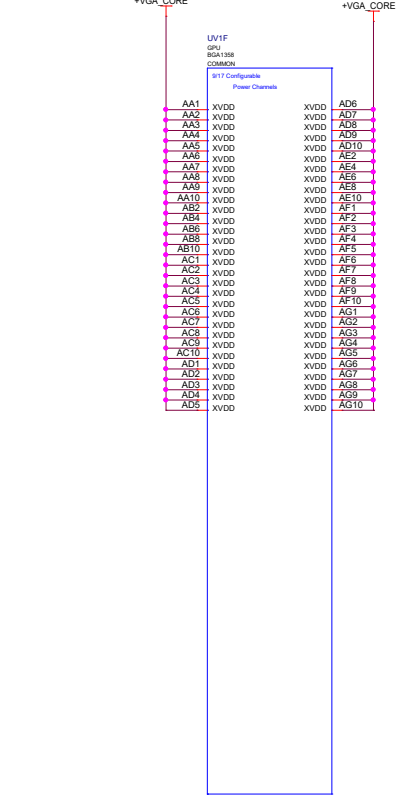
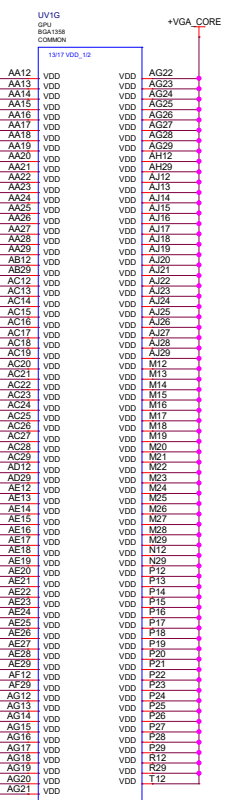
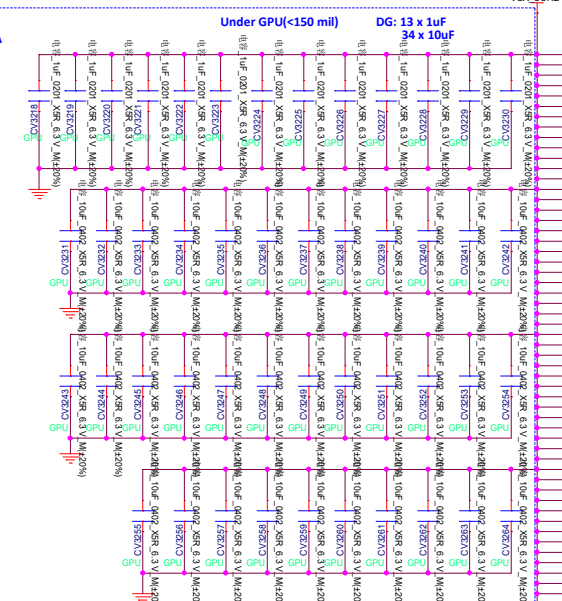
0.5A

FP FUSE /N18P ADD

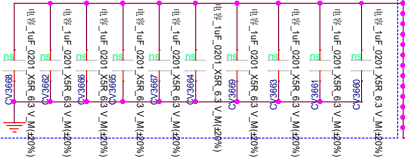




EDP 35A
Peak 150A

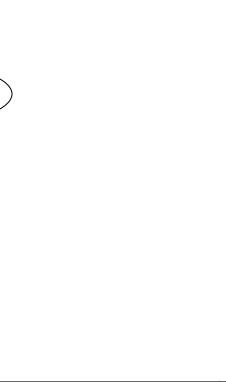
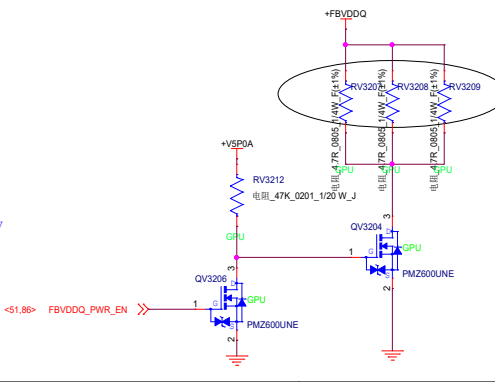
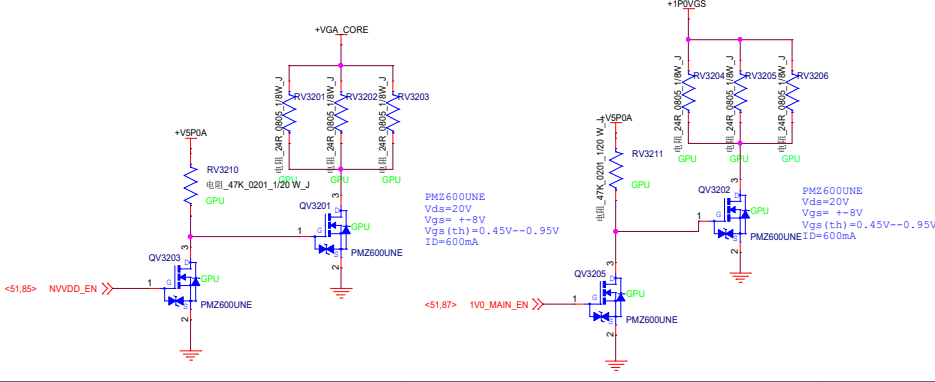


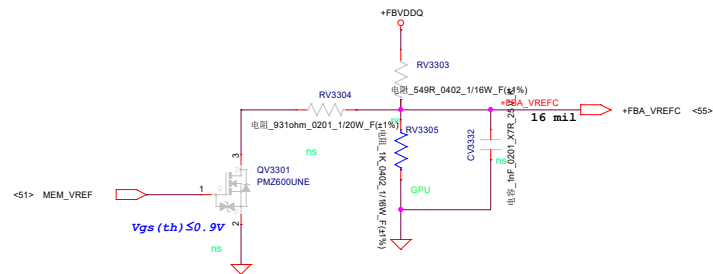
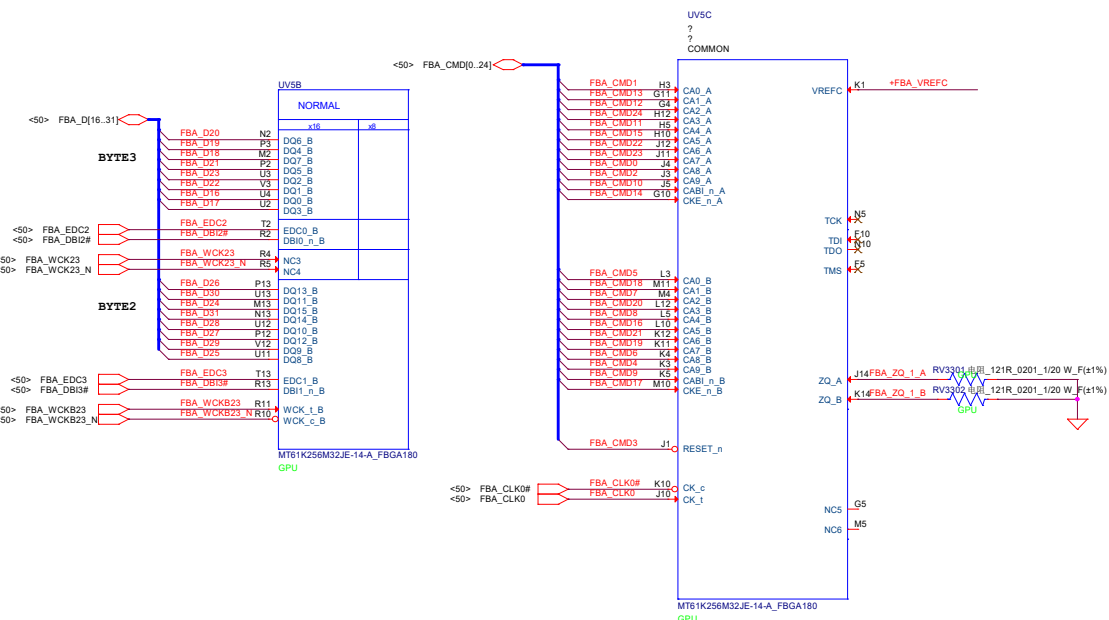
Under GPU
NV checklist: 10 x 1uF Reserve

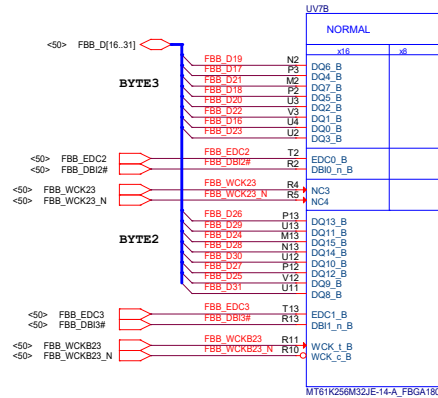
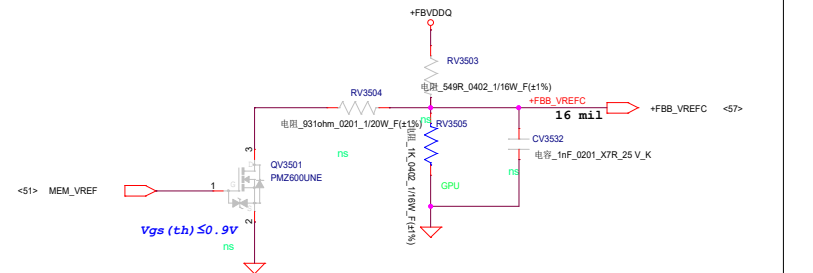



trace width: 16mils
differential voltage sensing.
differential signal routing.

PM2600UNE
Vds=20V
Vgs= ++8V
Vgs(th)=0.45V--0.95V
ID=600mA




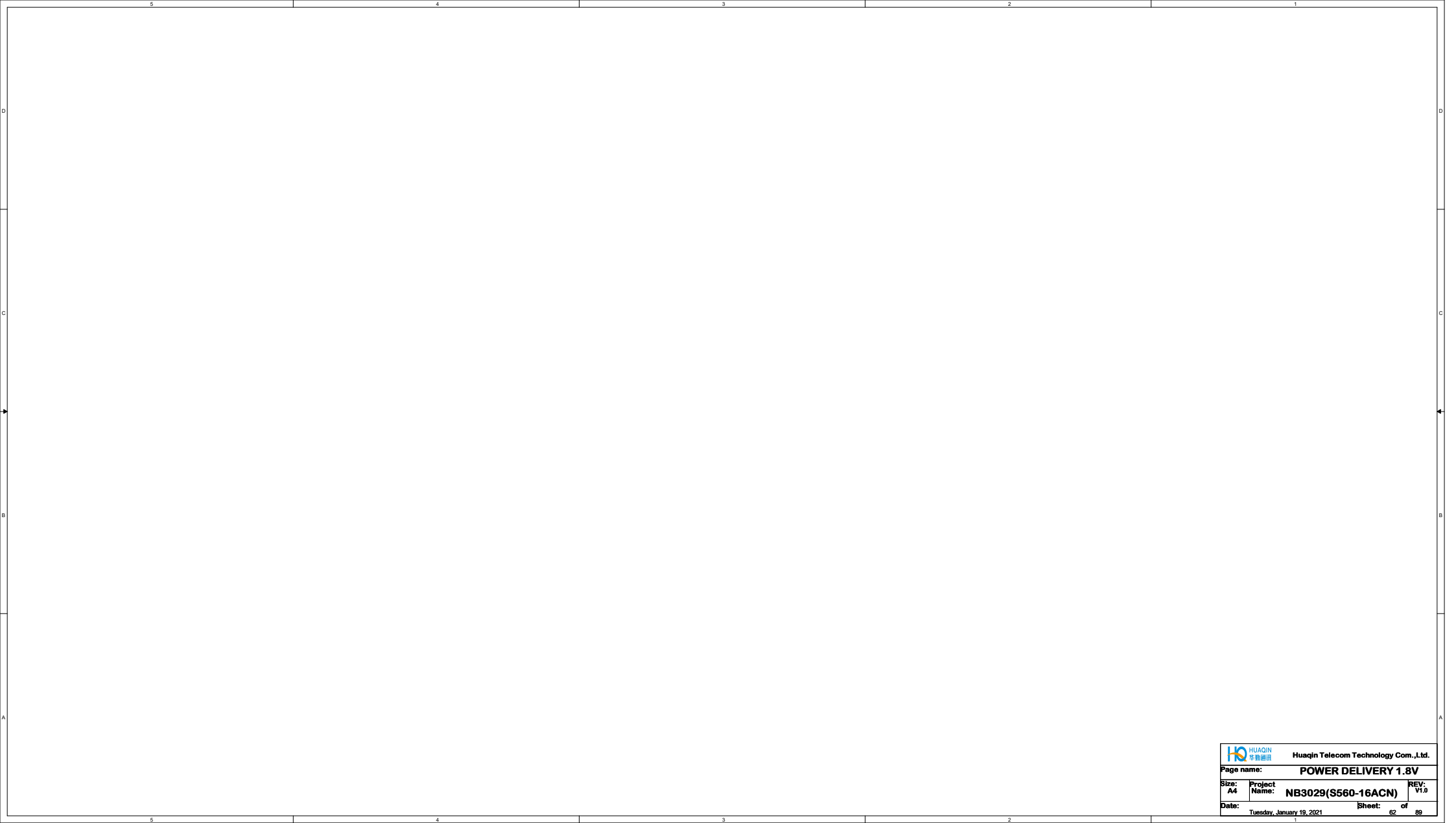



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		Huaqin Telecom Technology Co., Ltd.	
Page name: BLANK			
Size: A4	Project Name: NB3029(S560-16ACN)	REV: V1.0	
Date: Tuesday, January 10, 2021	Sheet: 56 of 80		

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

 Huaqin Telecom Technology Co., Ltd.		
Page name: POWER DELIVERY 3.3V		
Size: A4	Project Name: NB3029(S560-16ACN)	REV: V1.0
Date: Tuesday, January 19, 2021	Sheet: 60 of 89	

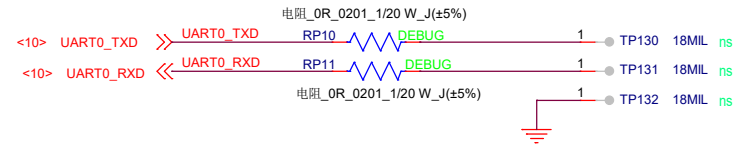
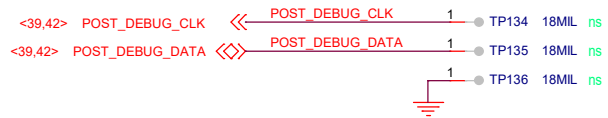
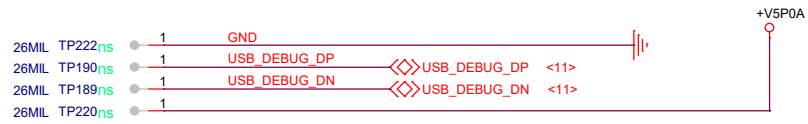



 HUAQIN 华勤通讯		Huaqin Telecom Technology Com.,Ltd.	
Page name:		POWER DELIVERY 1.8V	
Size: A4	Project Name:	NB3029(S560-16ACN)	REV: V1.0
Date:	Tuesday, January 19, 2021		Sheet: 62 of 89

 HUAQIN 华勤通讯		Huaqin Telecom Technology Co., Ltd.	
Page name:		POWER DELIVERY 0.75V	
Size: A4	Project Name: NB3029(S560-16ACN)	REV: V1.0	
Date: Tuesday, January 19, 2021	Sheet:	of	89



For product test



		Huaqin Telecom Technology Com.,Ltd.	
Page name: Debug Conn			
Size: A4	Project Name: NB3029(S560-16ACN)	REV: V1.0	
Date: Tuesday, January 19, 2021	Sheet: 65	of 89	



Huaqin Telecom Technology Com.,Ltd.

Page name:	Changelist
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Size:
A4

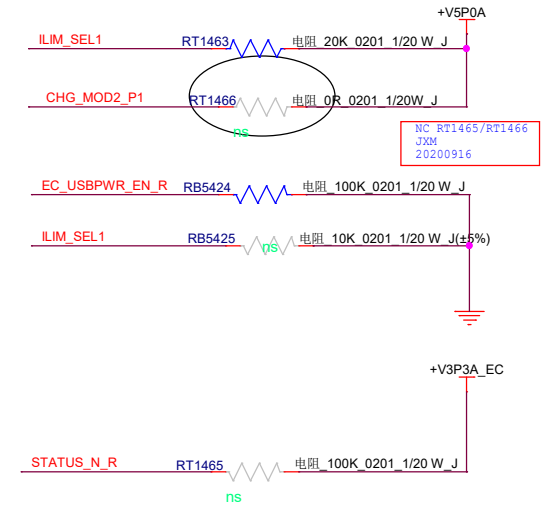
Project Name:	NB3029(S560-16ACN)
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REV:	V1.0
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Date: Tuesday, January 19, 2021

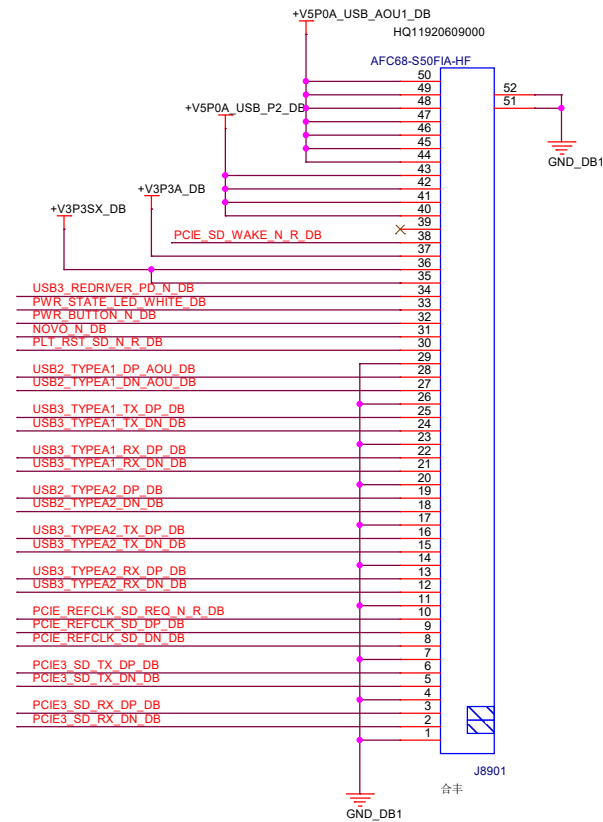
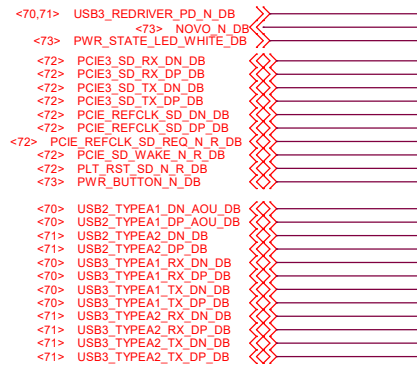
Sheet: 67 of 89

Power for TypeA Conn: 5V



To SOC



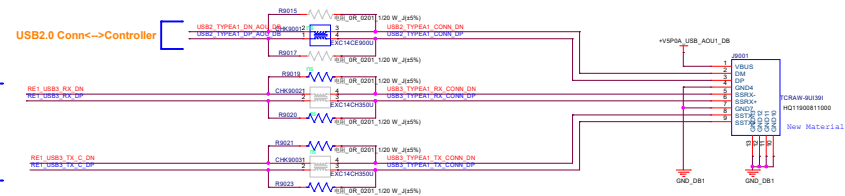


+60+ USB2_TYPA1_DN_AOU_DB
 +60+ USB2_TYPA1_DP_AOU_DB
 +60.70+ USB3_TYPA1_RX_DN_DB
 +60.70+ USB3_TYPA1_RX_DP_DB
 +60.70+ USB3_TYPA1_TX_DN_DB
 +60.70+ USB3_TYPA1_TX_DP_DB



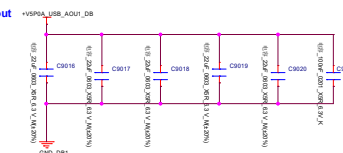
USB3.1 Conn<-->Redriver

USB2.0 Conn<-->Controller

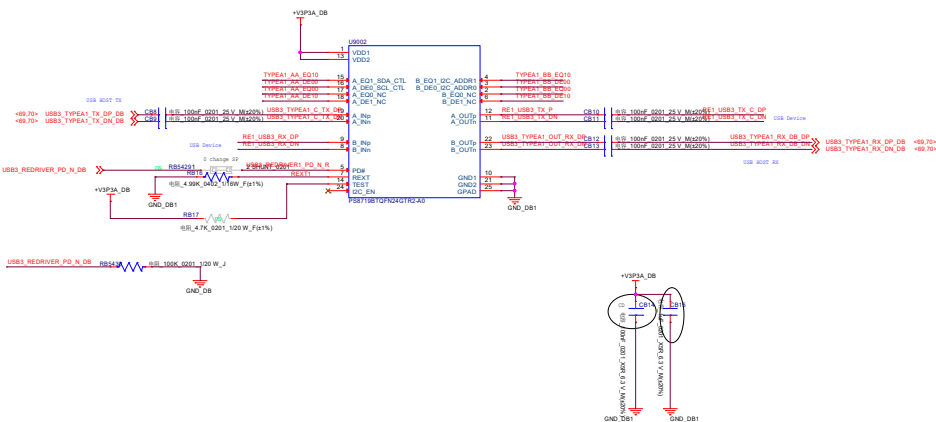


BYPASS CAPS

Close Conn@Layout
5V@2.2A

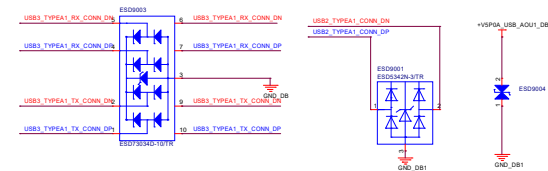


Type-A USB3.1 Gen1_Redriver

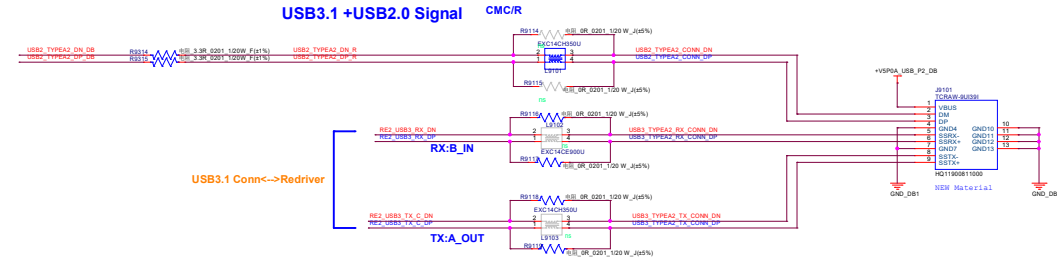


USB3.1 ESD

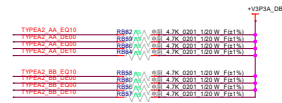
Close Conn@Layout



+69.71+ USB3_1TYPEA2_RX_DN_DB
 +69.71+ USB3_1TYPEA2_RX_DP_DB
 +69.71+ USB3_1TYPEA2_TX_DN_DB
 +69.71+ USB3_1TYPEA2_TX_DP_DB
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 +69.71+ USB3_1TYPEA2_TX_DP_DB

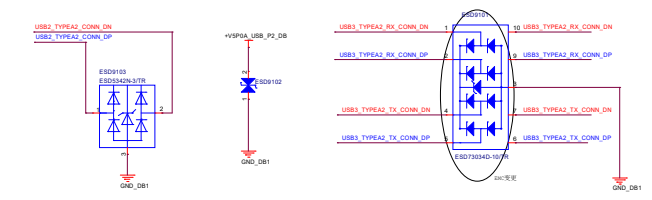


Redriver

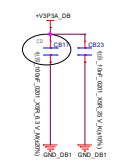
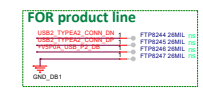
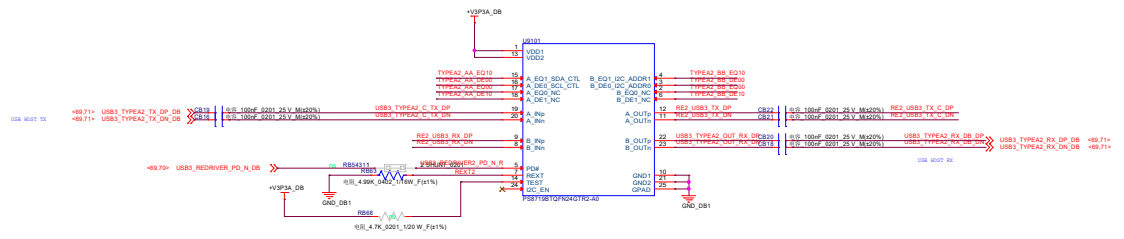


USB3.1 ESD For Gen1

Close to Conn



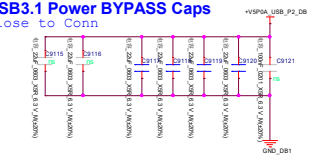
Type-A USB3.1 Gen1_Redriver

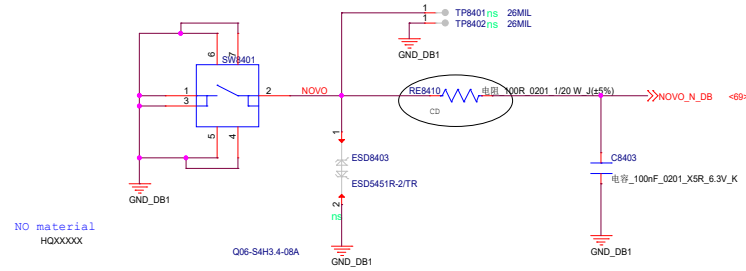


USB3.1 CONN For Gen1

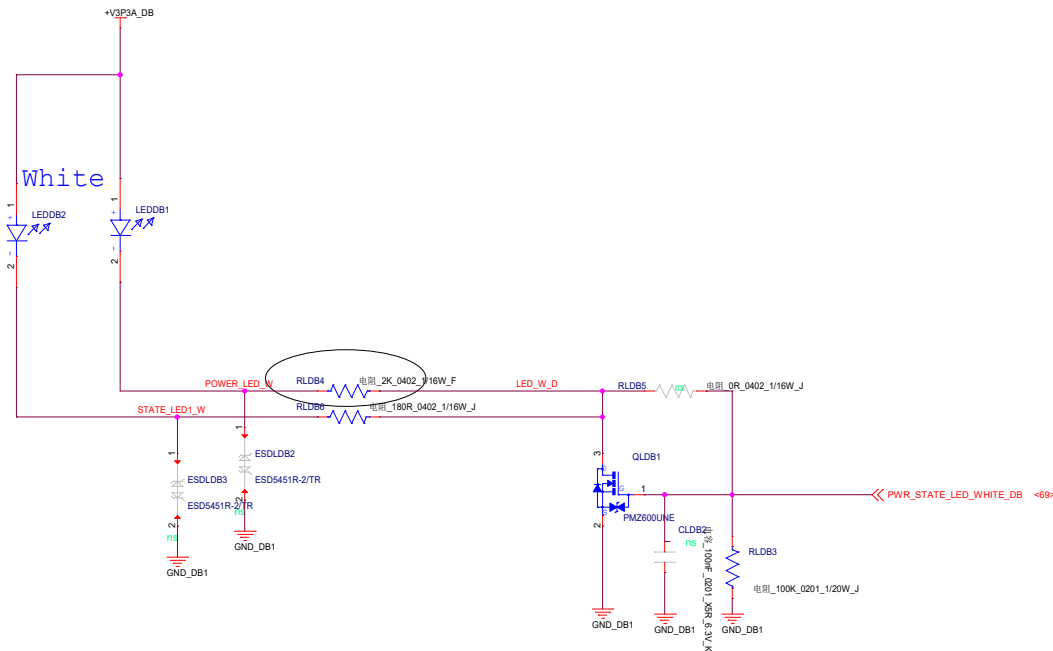
USB3.1 Power BYPASS Caps

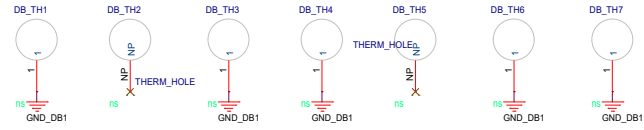
Close to Conn



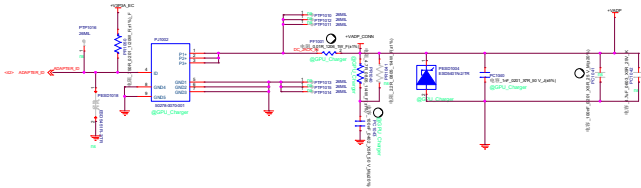


POWER LED : LEDDB2



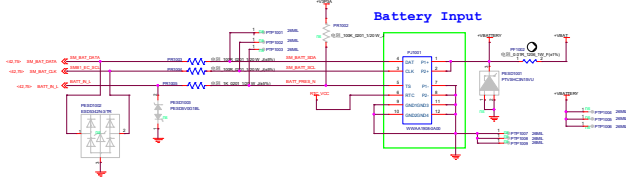
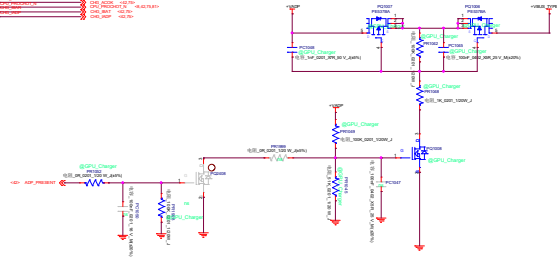


10 Pin Configure					
适配器电压	12V Adapter	9V Adapter	5V Adapter	4.5V Adapter	
ID Pin Voltage	10.0~1.0	9.0~1.0	5.0~1.0	4.5~1.0	
充电电压	10.0~1.0	9.0~1.0	5.0~1.0	4.5~1.0	
充电电流	0.0~1.0	0.0~1.0	0.0~1.0	0.0~1.0	
INPUT CURRENT SETTING (mA)	0.0	0.0	0.0	0.0	0.0



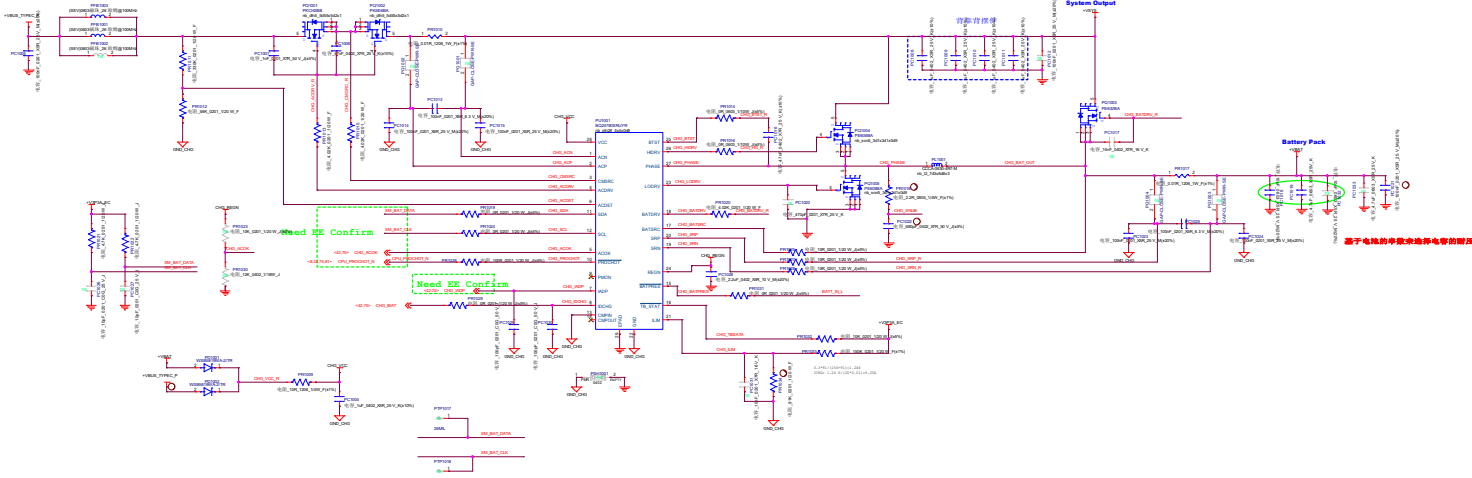
8000 Charger
需要上电
才能正常工作

BAT_VDDA
BAT_VDD
BAT_VDD2
BAT_VDD3
BAT_VDD4
BAT_VDD5
BAT_VDD6
BAT_VDD7
BAT_VDD8
BAT_VDD9
BAT_VDD10



Charger

Charger



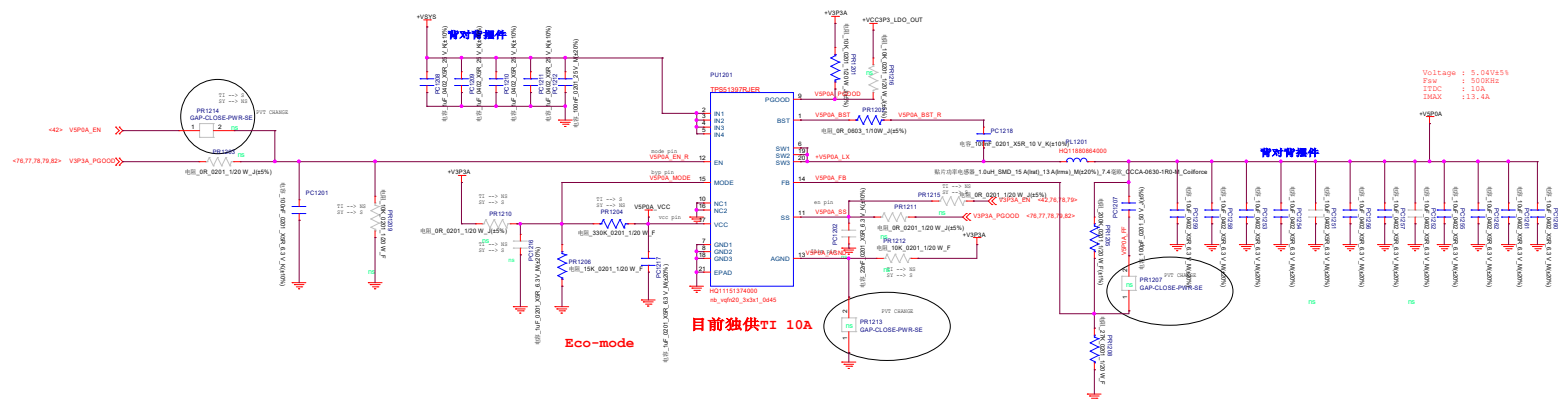
change0818

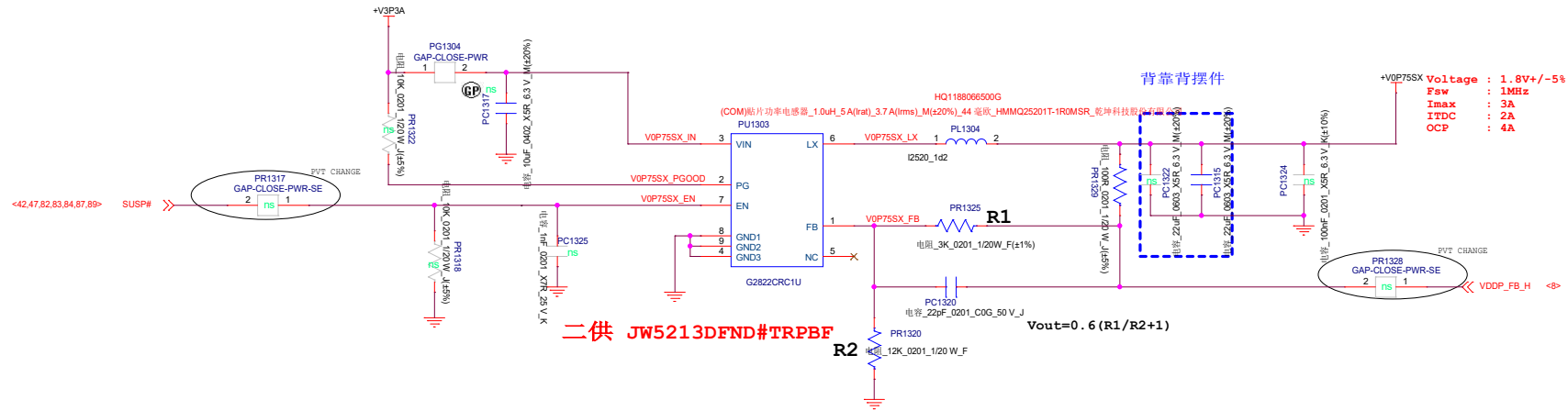
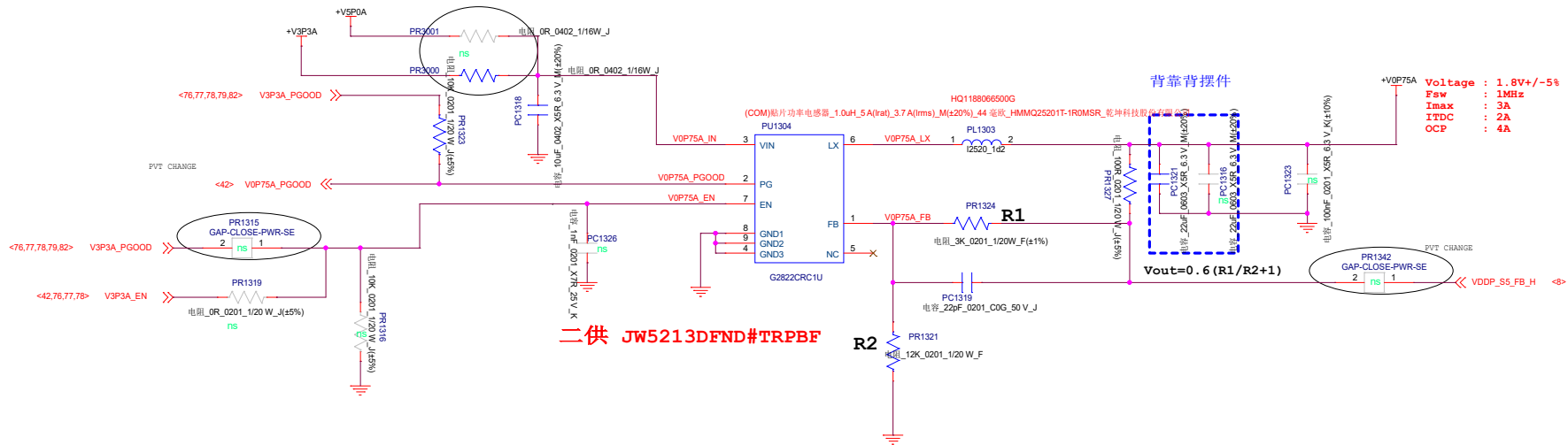
[illegible]

独供




Voltage : 3.3V±5%
Fsw : 625KHz
ITDC : 8A
OCP : 9.6A

change0818

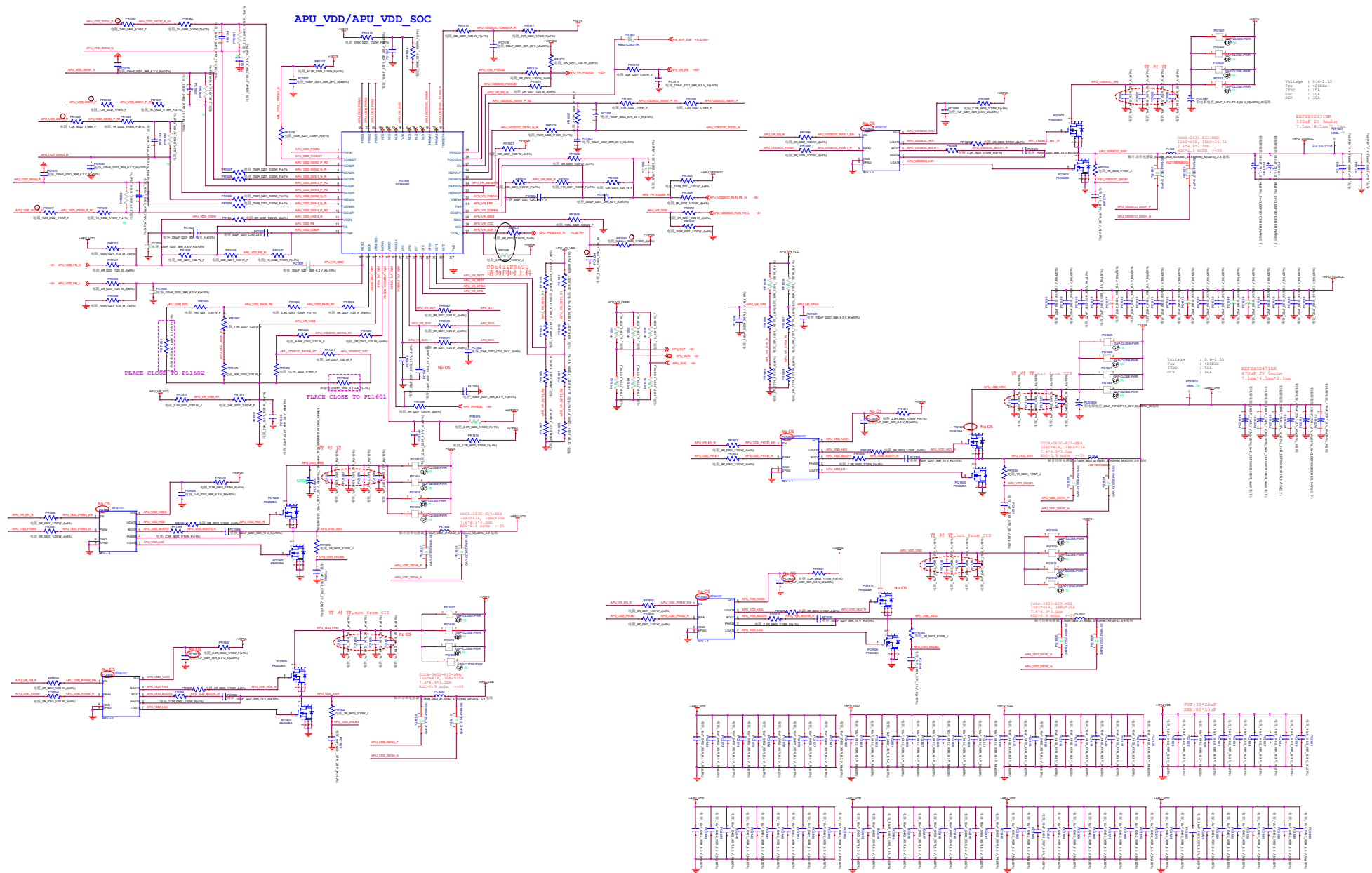


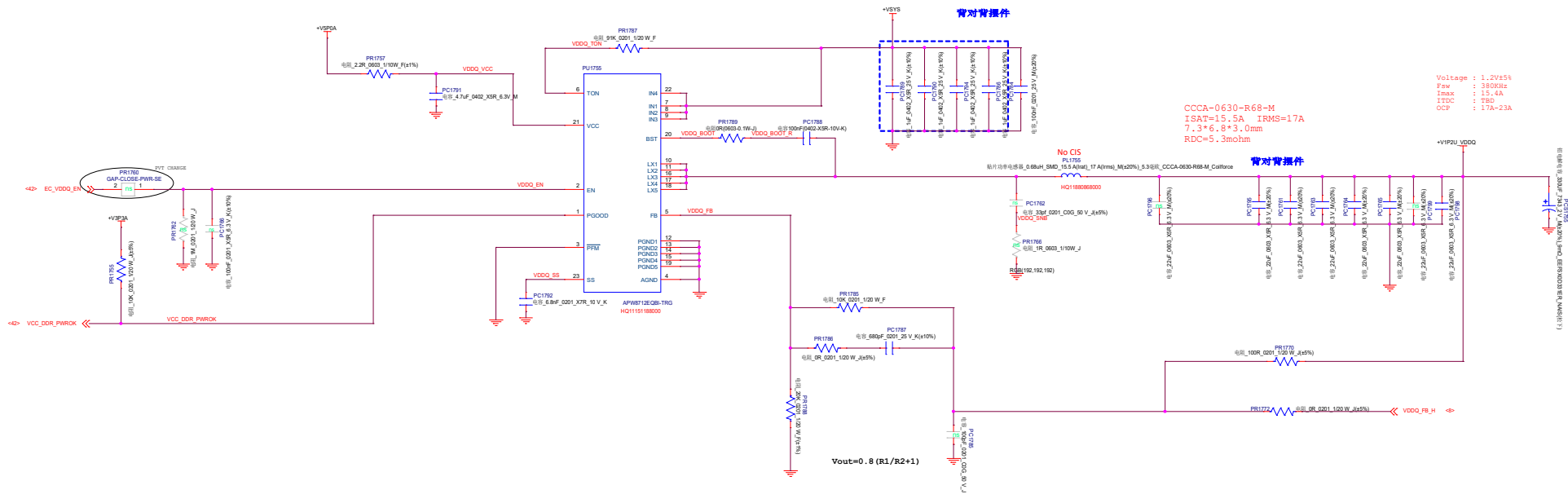


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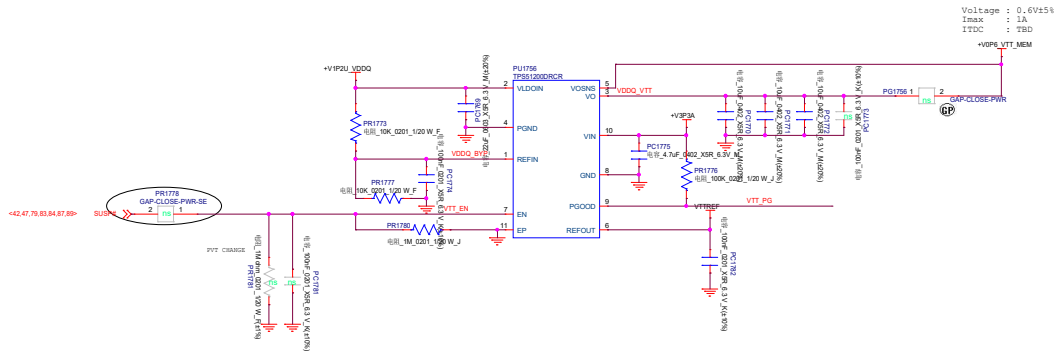
5					4					3					2					1																																																																															
D																																																																																																			
C																																																																																																			
B																																																																																																			
A																																																																																																			
															<table><tr><td colspan="5"></td><td colspan="5">Huaqin Telecom Technology Com.,Ltd.</td></tr><tr><td colspan="20">Page name: BLANK</td></tr><tr><td colspan="3">Size: A4</td><td colspan="14">Project Name: NB3029(S560-16ACN)</td><td colspan="3">REV: V1.0</td></tr><tr><td colspan="15">Date: Tuesday, January 19, 2021</td><td colspan="10">Sheet: 80 of 89</td></tr></table>															Huaqin Telecom Technology Com.,Ltd.					Page name: BLANK																				Size: A4			Project Name: NB3029(S560-16ACN)														REV: V1.0			Date: Tuesday, January 19, 2021															Sheet: 80 of 89									
					Huaqin Telecom Technology Com.,Ltd.																																																																																														
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Size: A4			Project Name: NB3029(S560-16ACN)														REV: V1.0																																																																																		
Date: Tuesday, January 19, 2021															Sheet: 80 of 89																																																																																				
5					4					3					2					1																																																																															

change0818

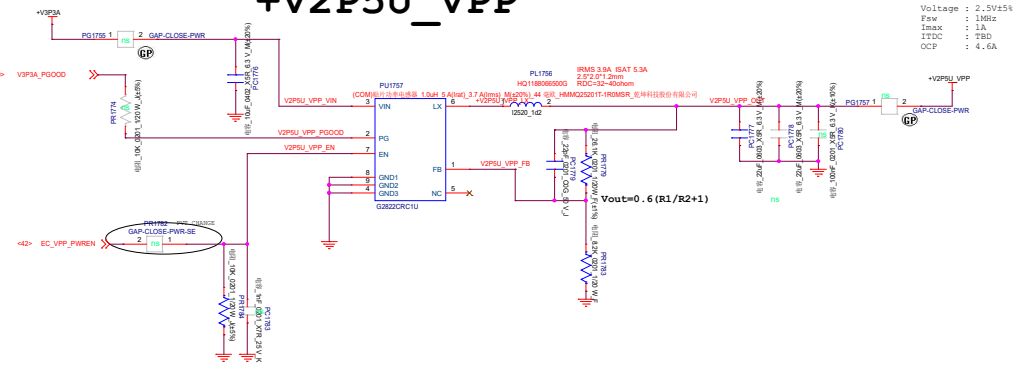




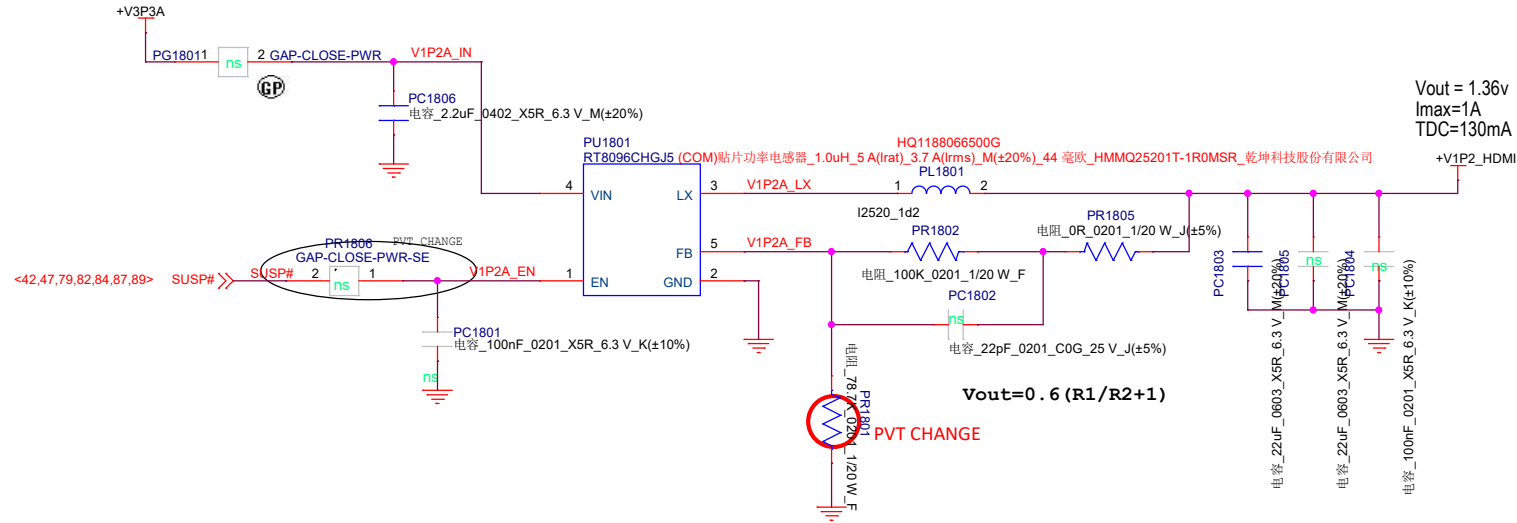
VTT



+V2P5U_VPP

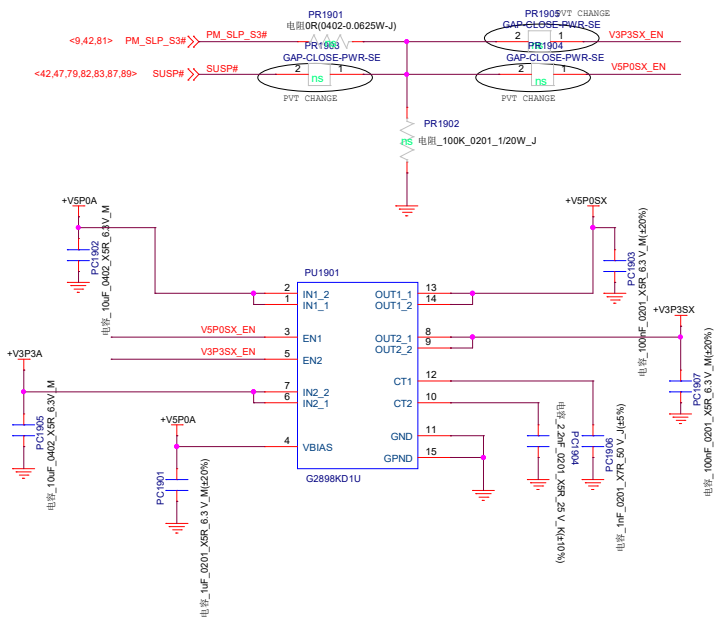


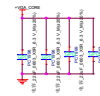
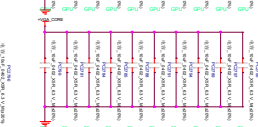
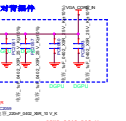
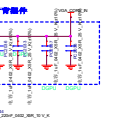
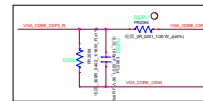
change1002



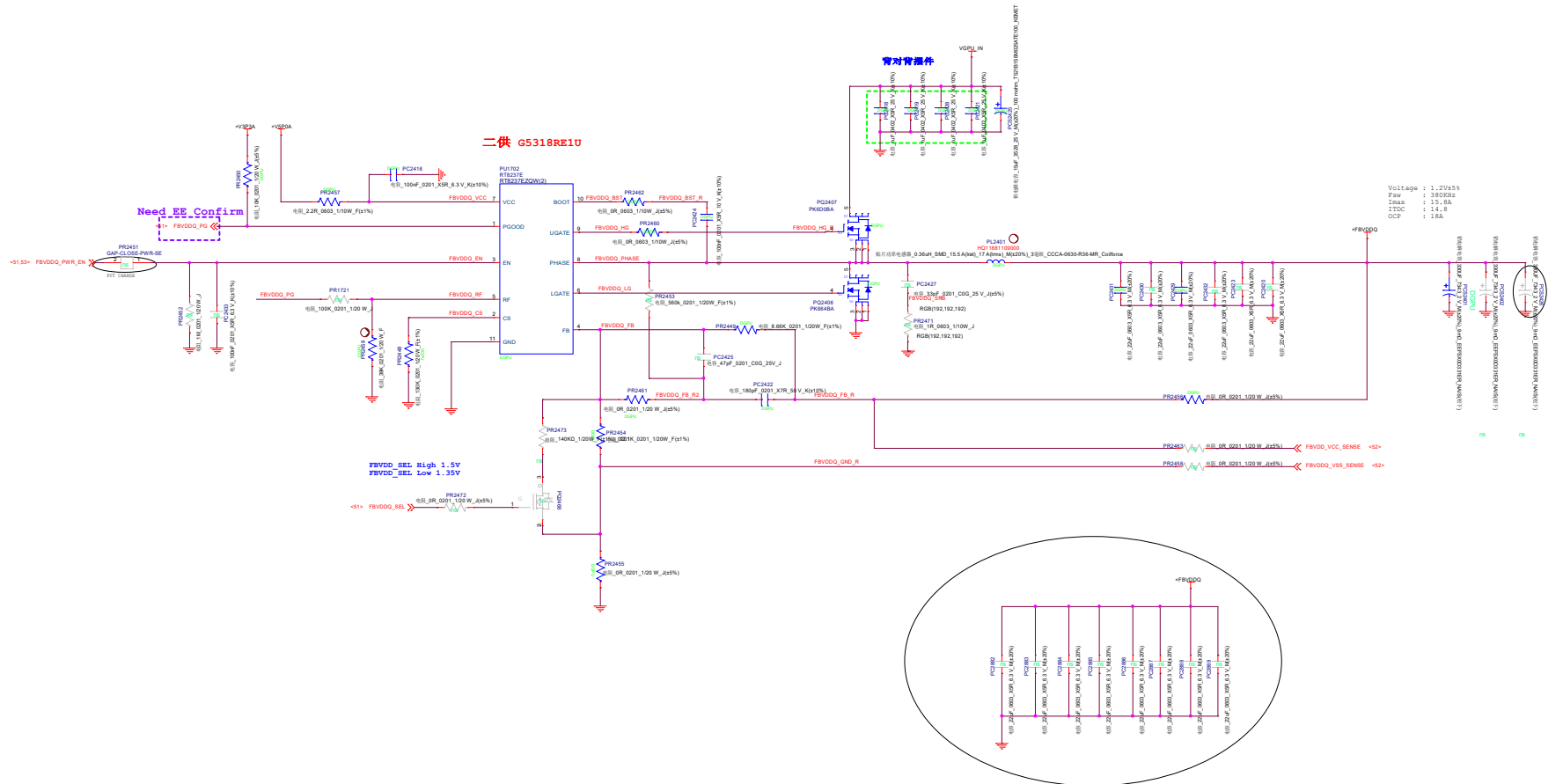
change0818

+V3P3SX, +V5P0SX G2898



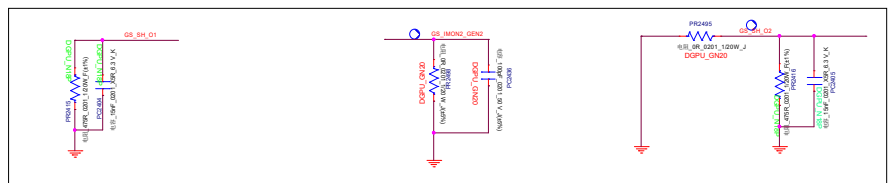
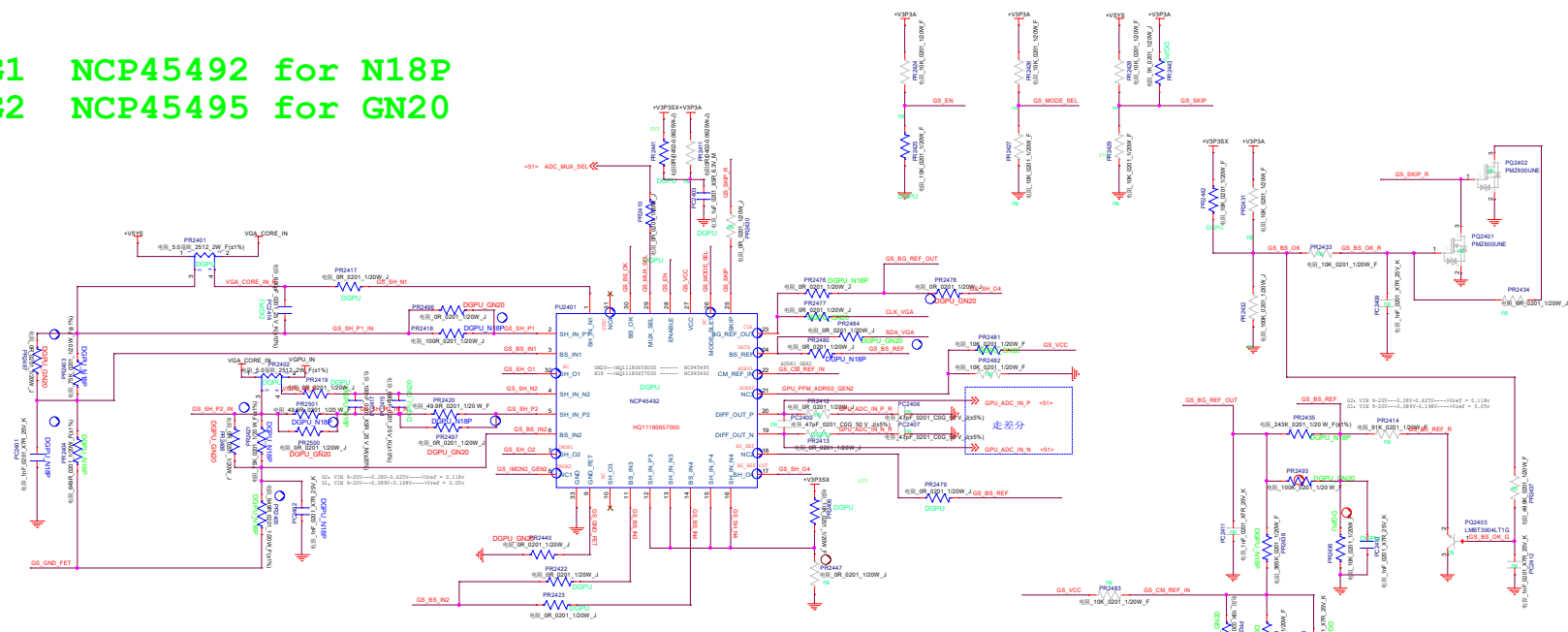


change0818



change0818

G1 NCP45492 for N18P
G2 NCP45495 for GN20



8 bits I2C address listed below

ADDR1	ADDR0	Device Address
0	0	0x58
0	1	0x5A
1	0	0x5C
1	1	0x5E

change0818

